

Compal Confidential

ZRMAA/ZEMAA Schematics Document

Haswell ULT with DDR3L

nVIDIA N14P-GV2 (Dual Rank)

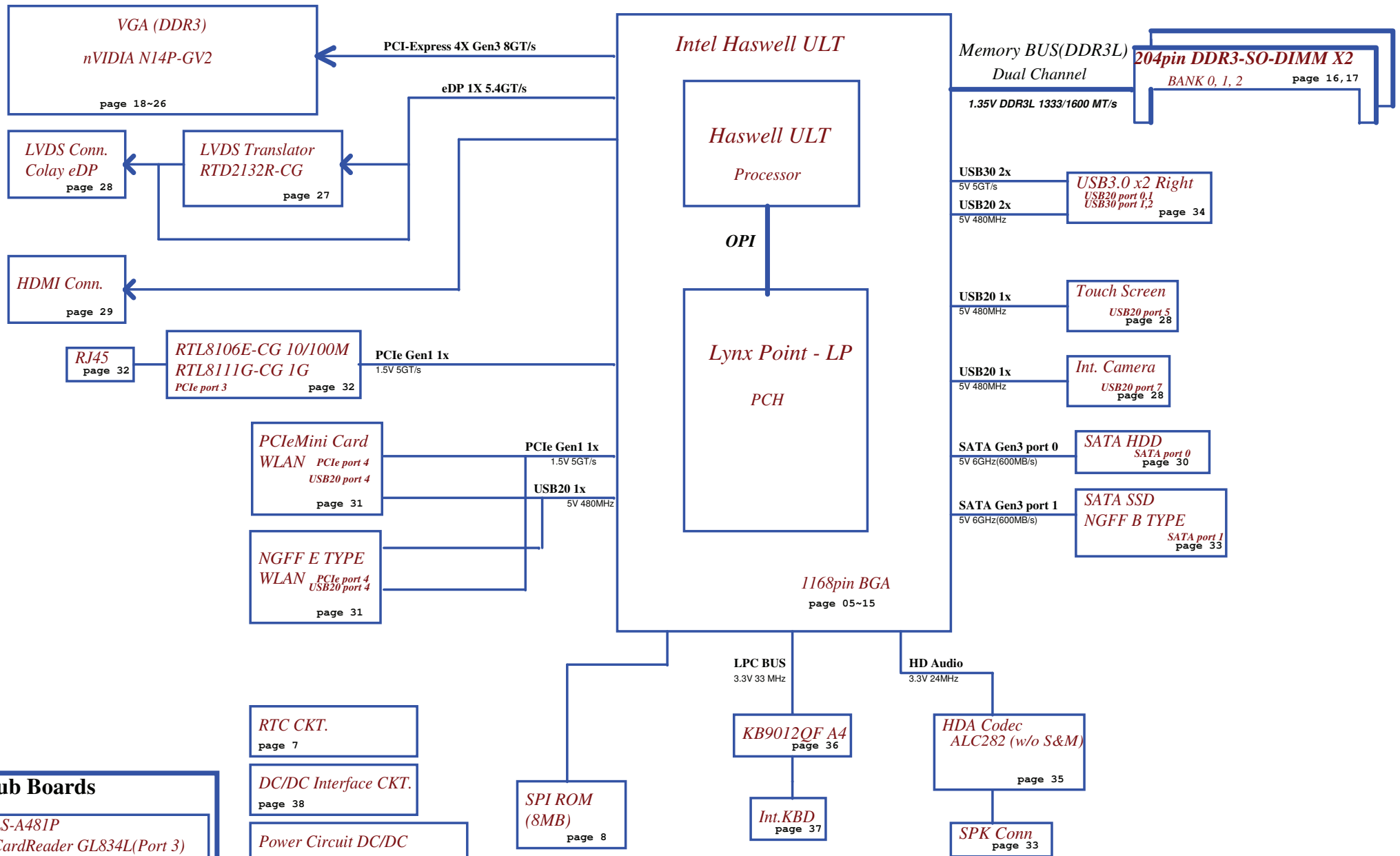
nVIDIA N14M-GL

LA-A481P REV 1.0 Schematic

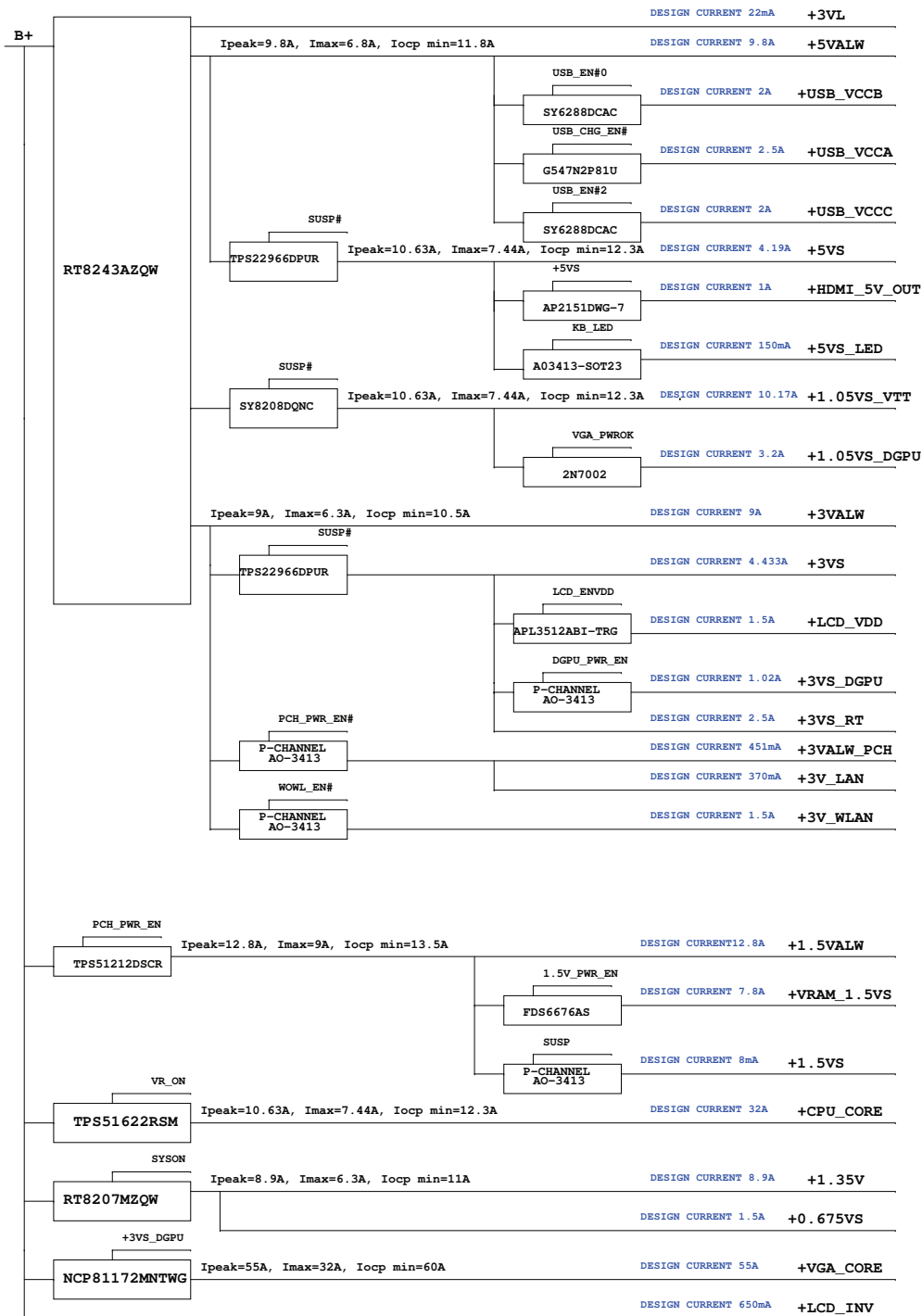
Intel Processor (Haswell)

2013-06-21 Rev 1.0

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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	Cover Page
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.5VALW +VSB	+1.35V	+5VS +3VS +1.8VS_CRT +1.5VS +CPU_CORE +VGA_CORE +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU +1.05VS_VTT
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b

Platform	SKU	CPU	PCH	VGA
				nVIDIA N13P-GL (N13PGL@)

BTO Option Table

Function	SKU	MIC	LAN			
description						
explain						
BTO						

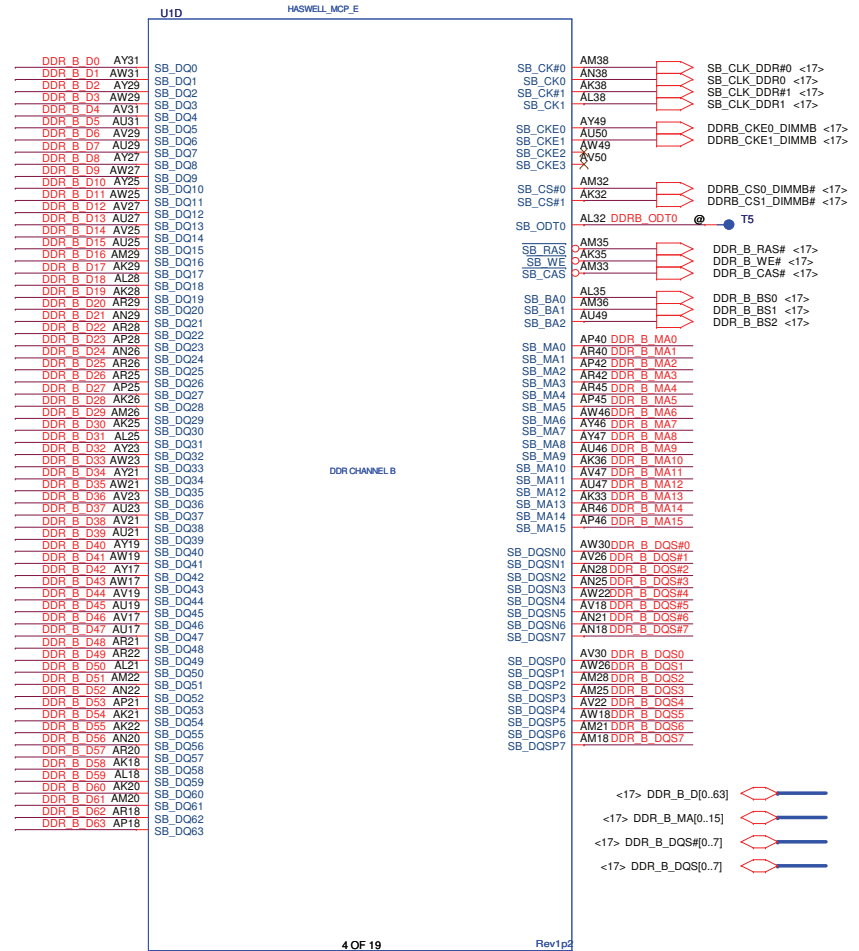
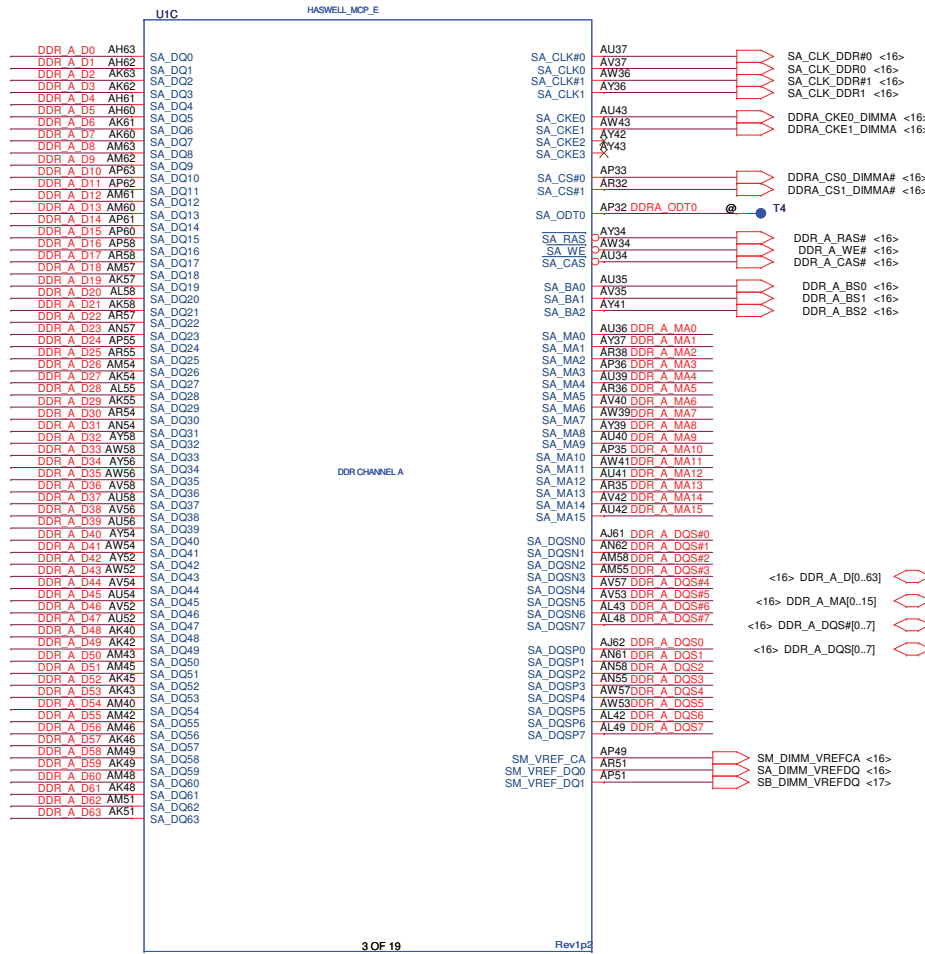
Function						
description						
explain						
BTO						

Function						
description						
explain						
BTO						

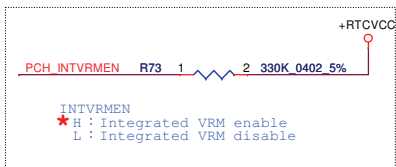
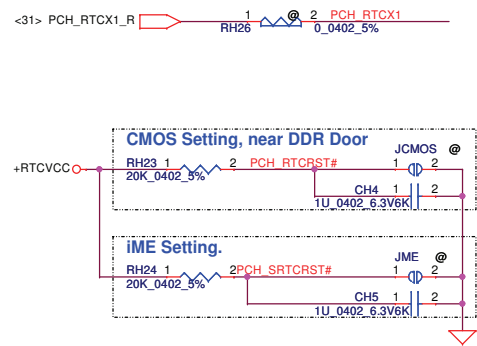
Function		
description		
explain		
BTO		

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

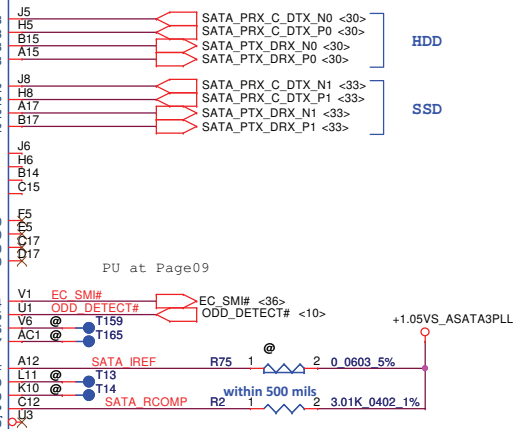
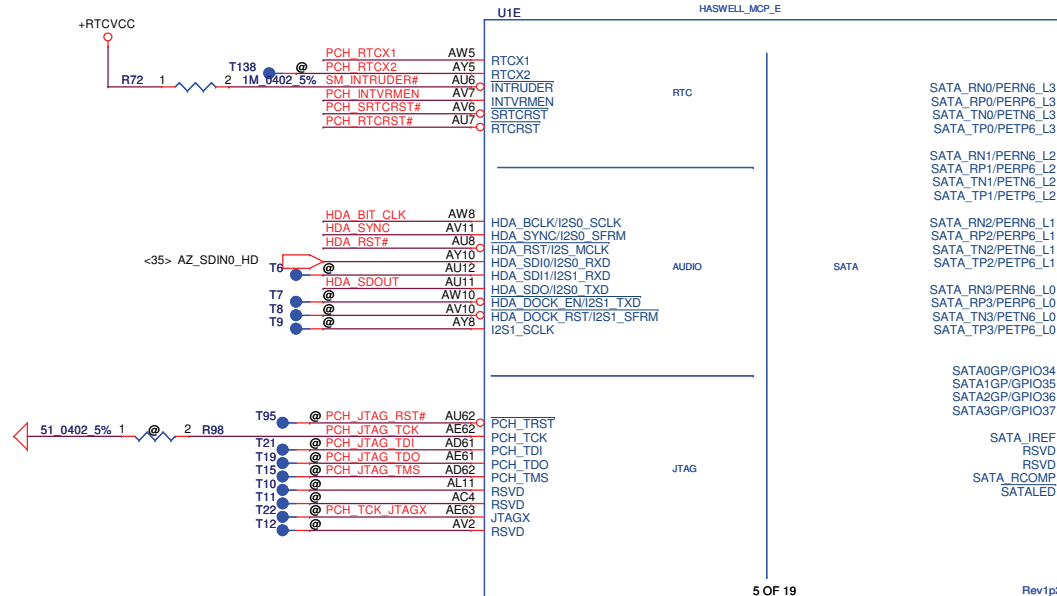
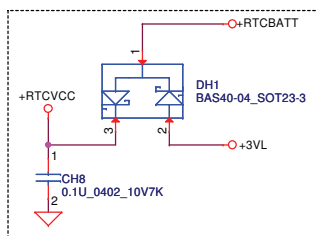
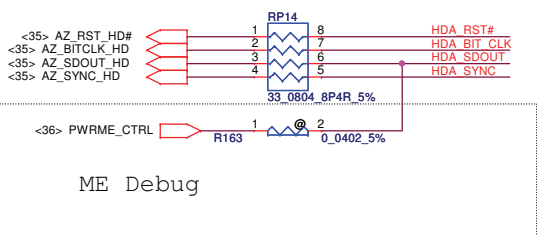
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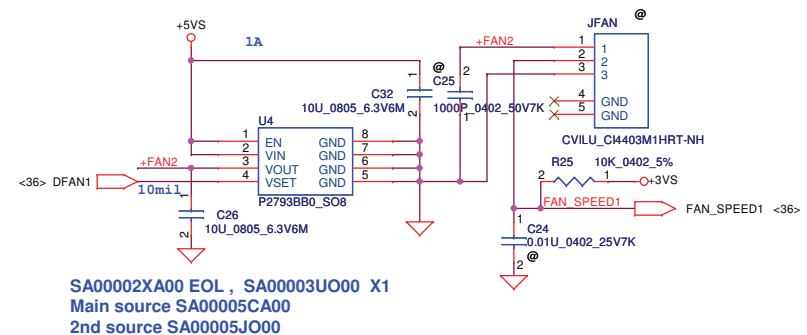
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	HSW MCP(2/11) DDRIII
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HDA for AUDIO



FAN Control Circuit

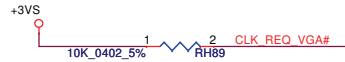


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PCIE LAN

WLAN

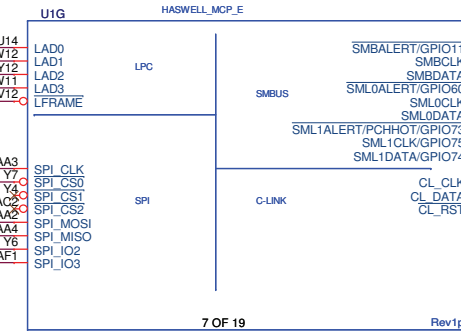


<36> LPC_AD0
<36> LPC_AD1
<36> LPC_AD2
<36> LPC_AD3
<36> LPC_FRAME#

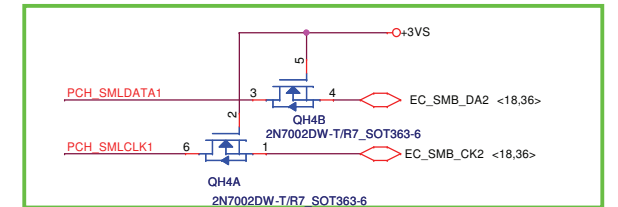
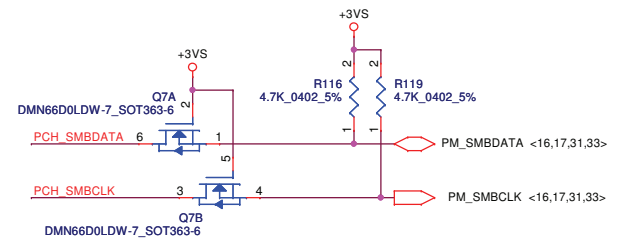
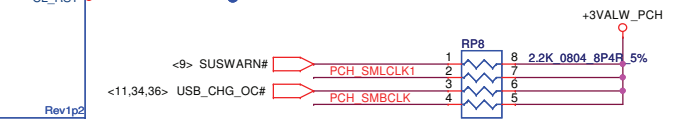
PCH SPICLK
PCH SPICS0#
PCH SPIDI
PCH SPIDO1
PCH SPIDO2
PCH SPIDO3



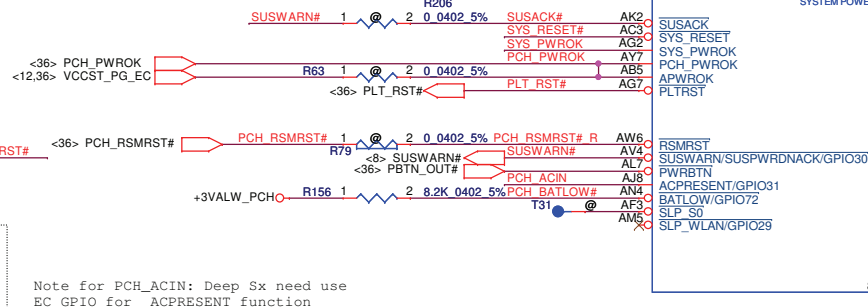
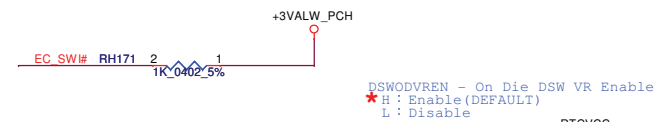
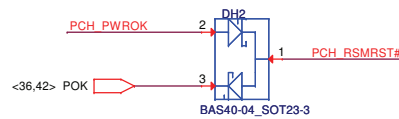
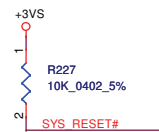
Socket: SP07000F500/SP07000H900
Please place UH3 close to U1 CPU,
Please place RH66, RH67, RH68 near UH3



AN2 PCH SMBCLK
AP2 PCH SMBDATA
AH1 PCH SMBDATA
AL2 LAN_EN <10,32>
AN1 SMLCLK <10>
AK1 SMLDATA <10>
AU4 PCH SMLCLK1
AU3 PCH SMLDATA1 <10>
AF2 PU 2.2K at EC side (+3VS)
AD2
AF4

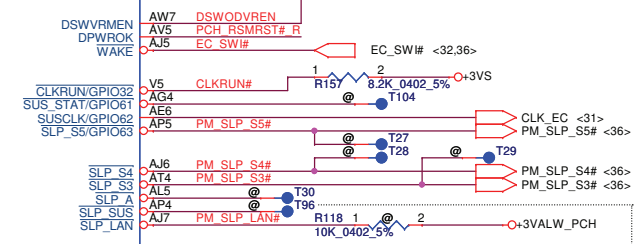


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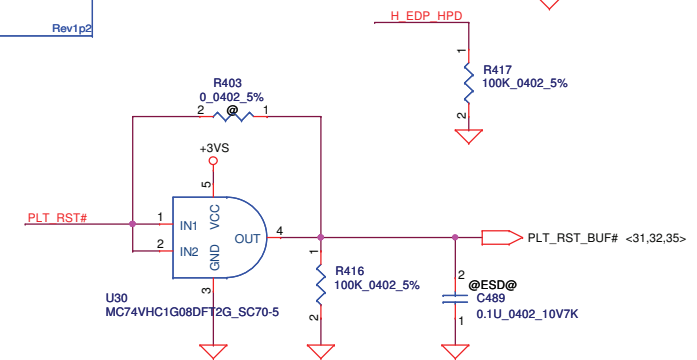
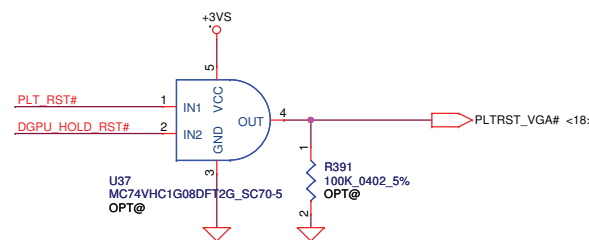
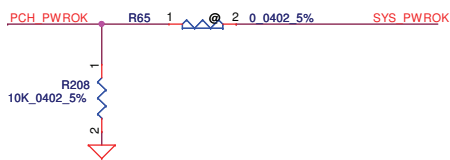
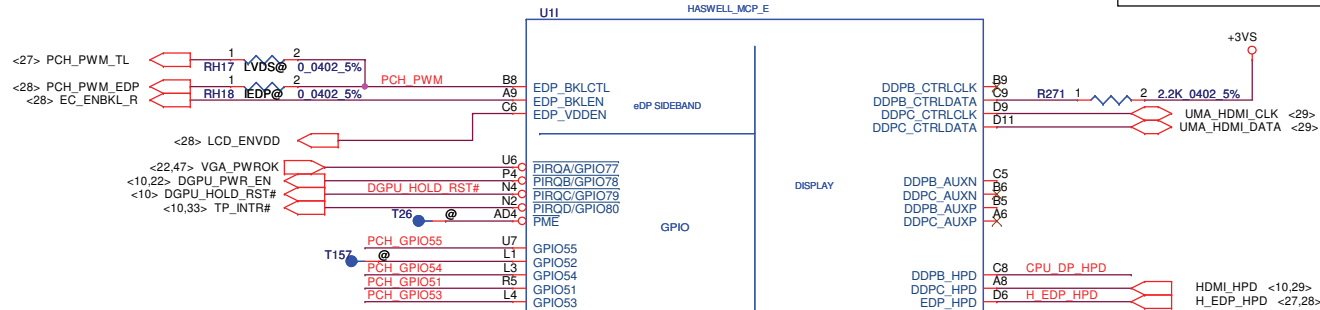
Note for PCH_ACIN: Deep Sx need use EC GPIO for ACPRESENT function

Need to Check



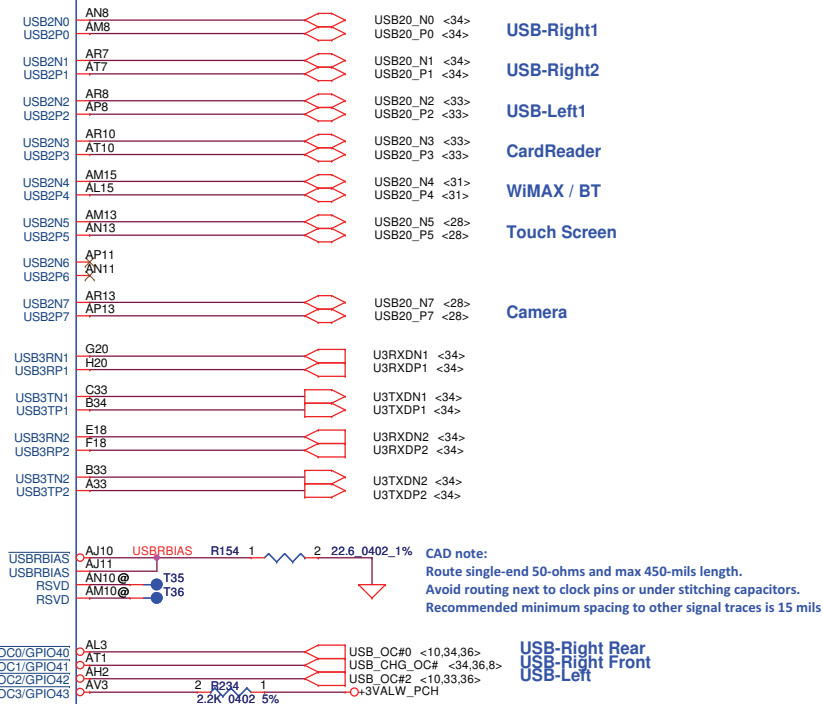
not support Deep S4,S5 can NC

DDPB_CTRLCLK: Port B Detected
DDPC_CTRLCLK: Port C Detected
* 1: Port B or C is detected
0: Port B or C is not detected
(Have internal PD)



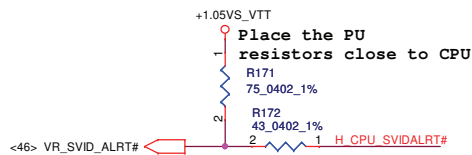
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2013/07/10		Title		HSW MCP(5/11) PM,GPIO,DDI	
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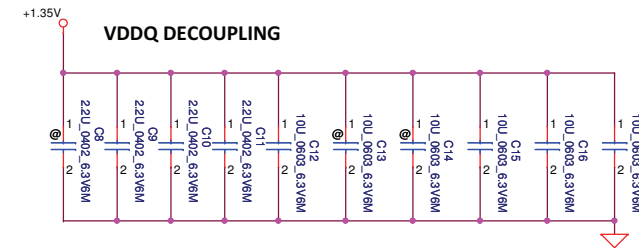
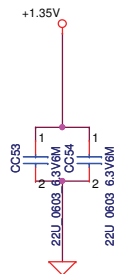
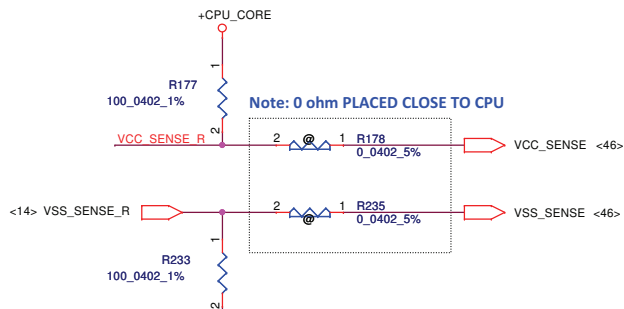
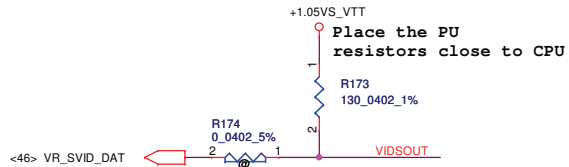


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SVID ALERT

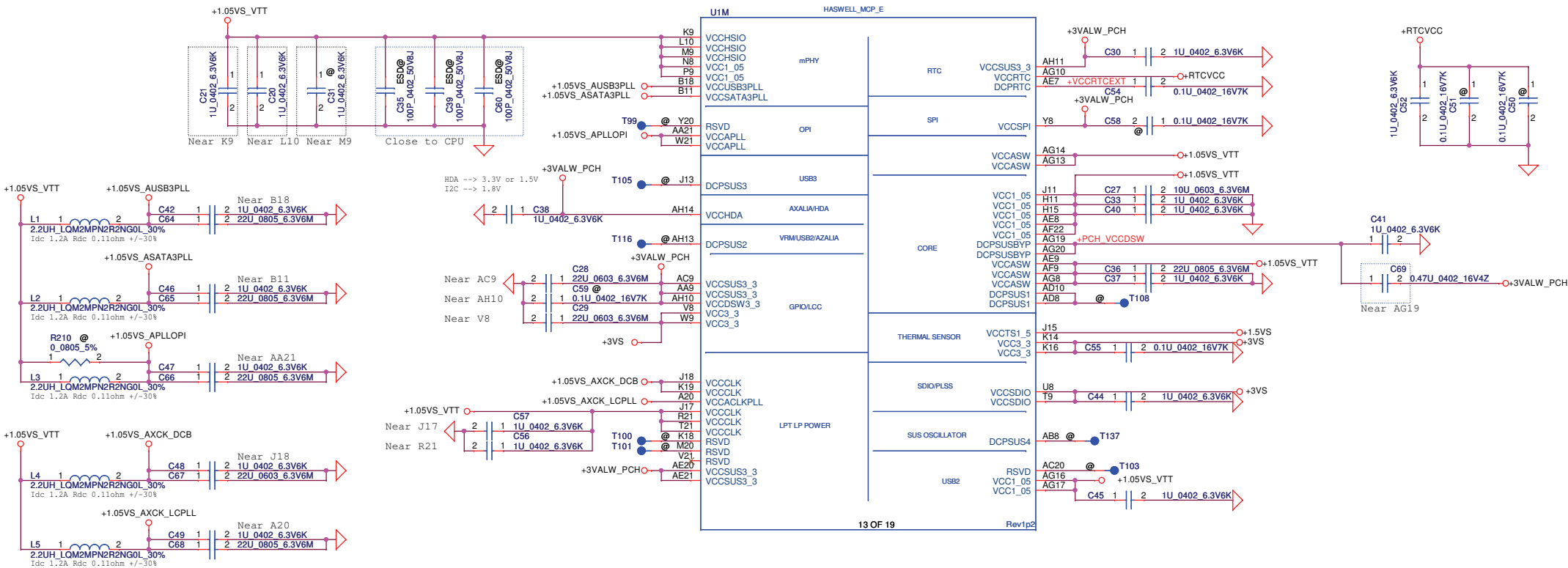


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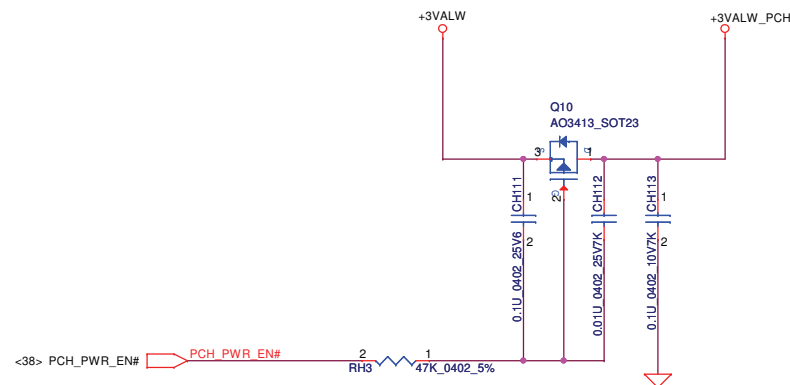


+1.35V : 470UF/2V/7343 *2
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4

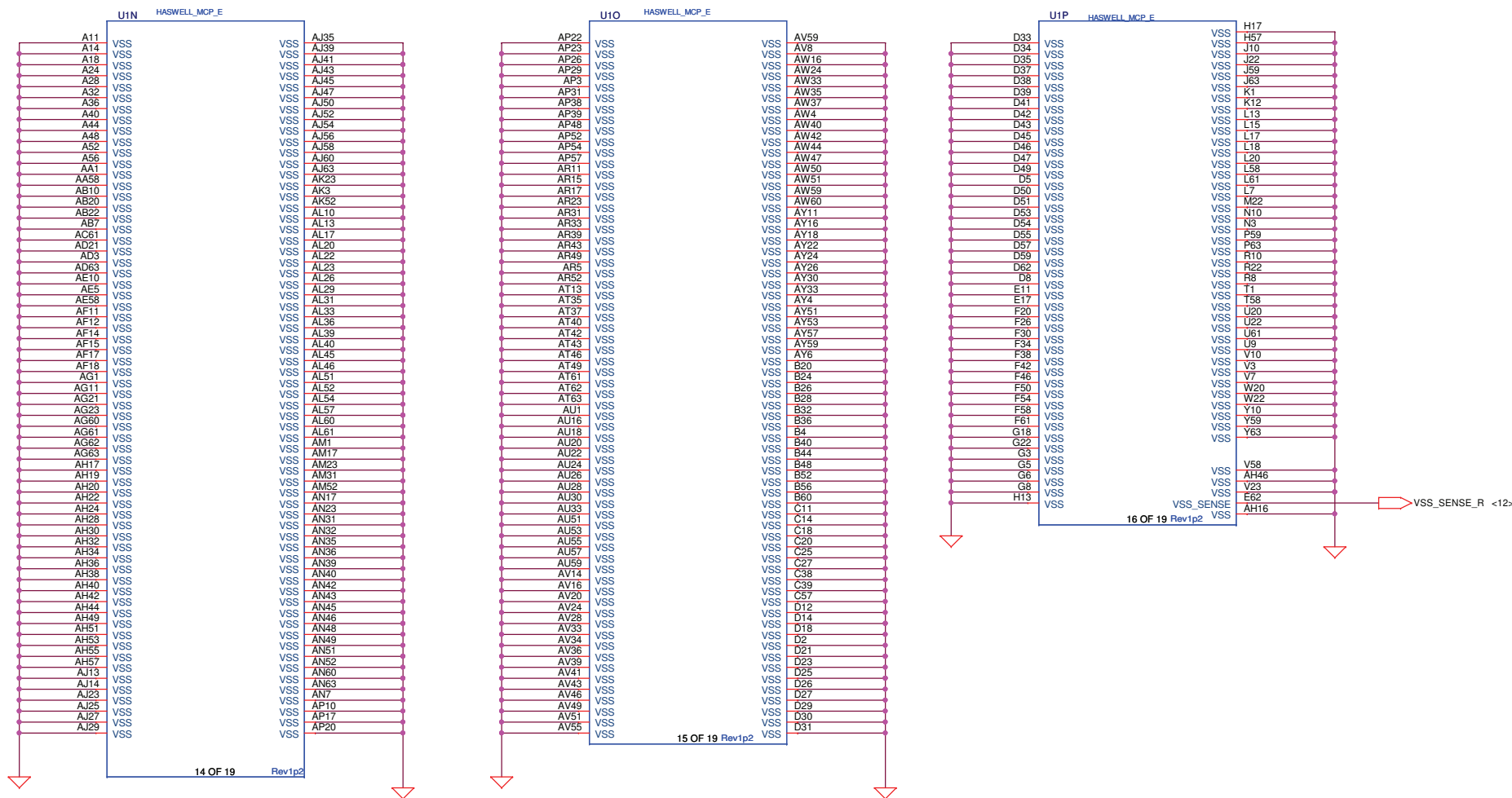
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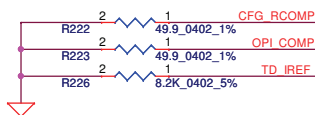
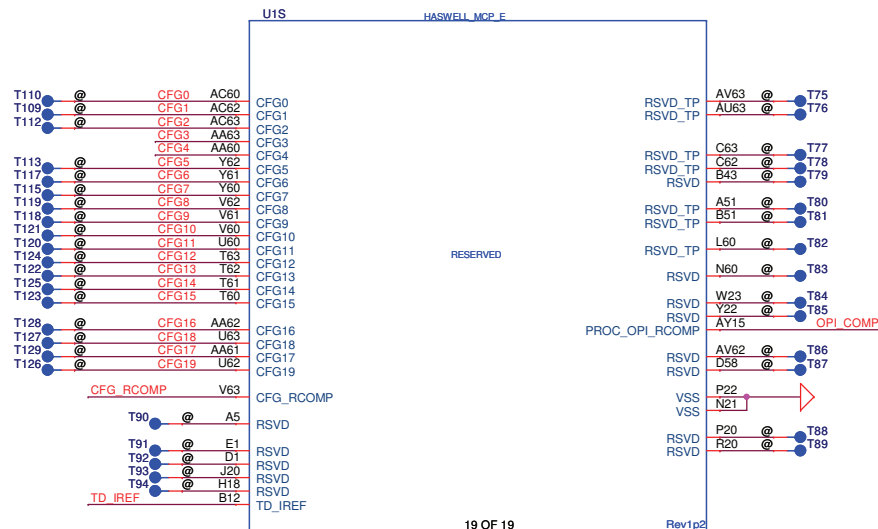
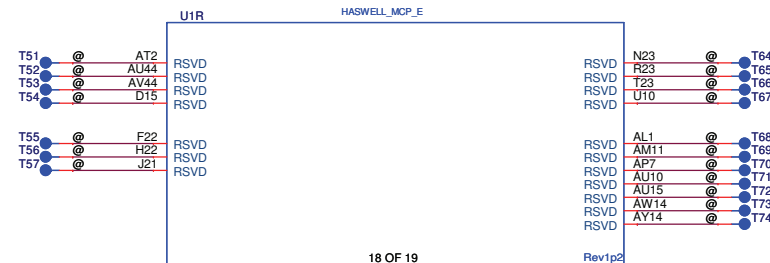
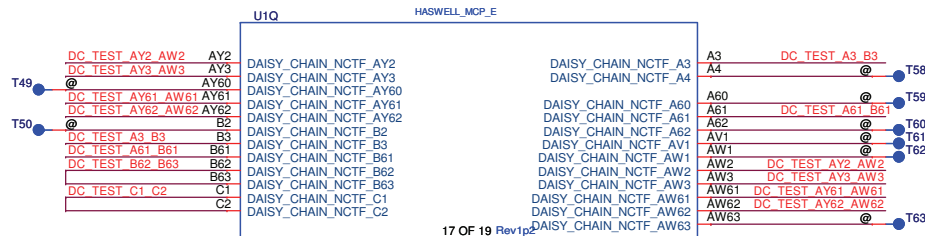
+3VALW to +3VALW_PCH



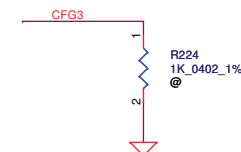
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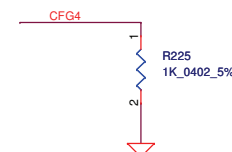
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CFG Straps for Processor

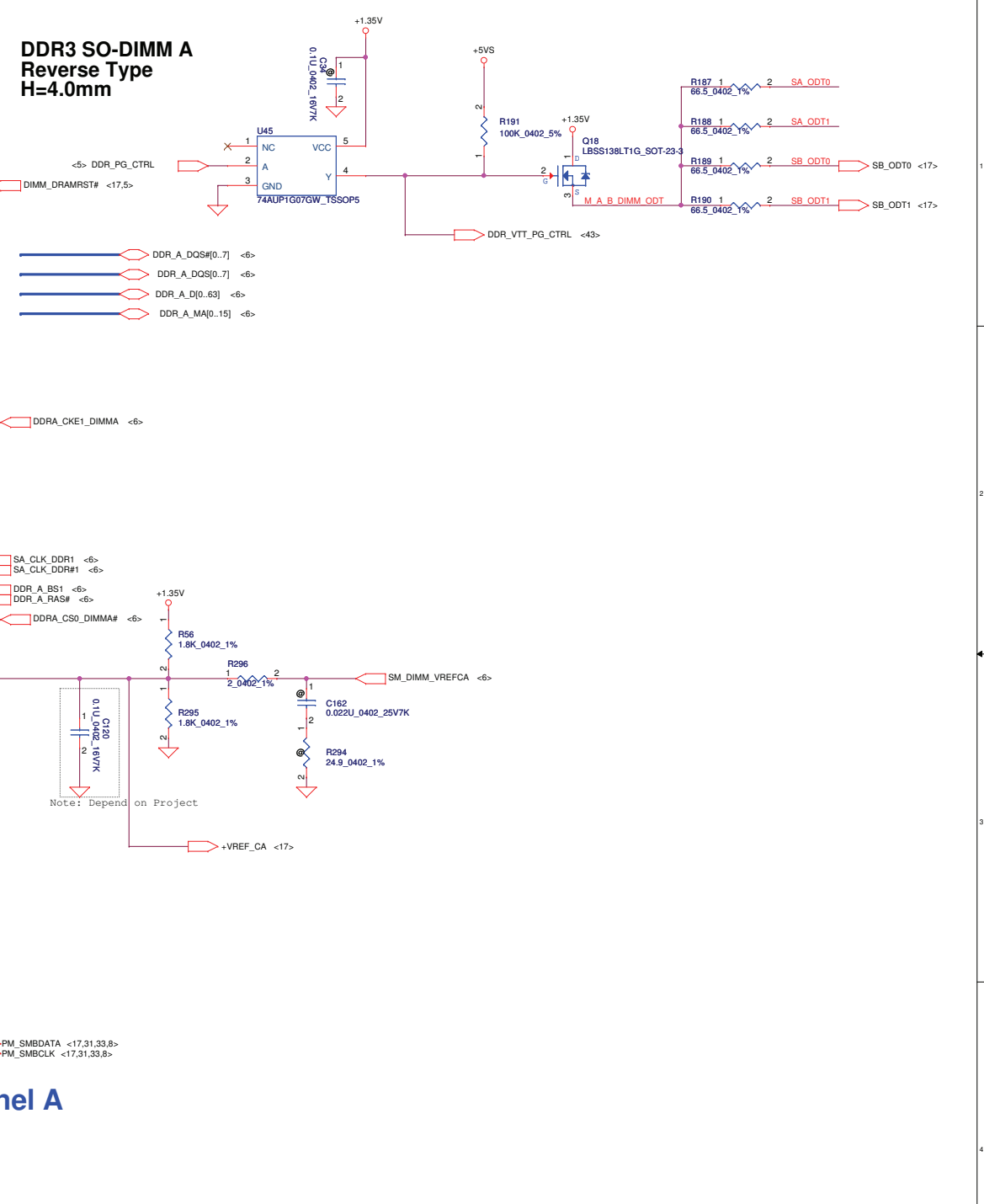
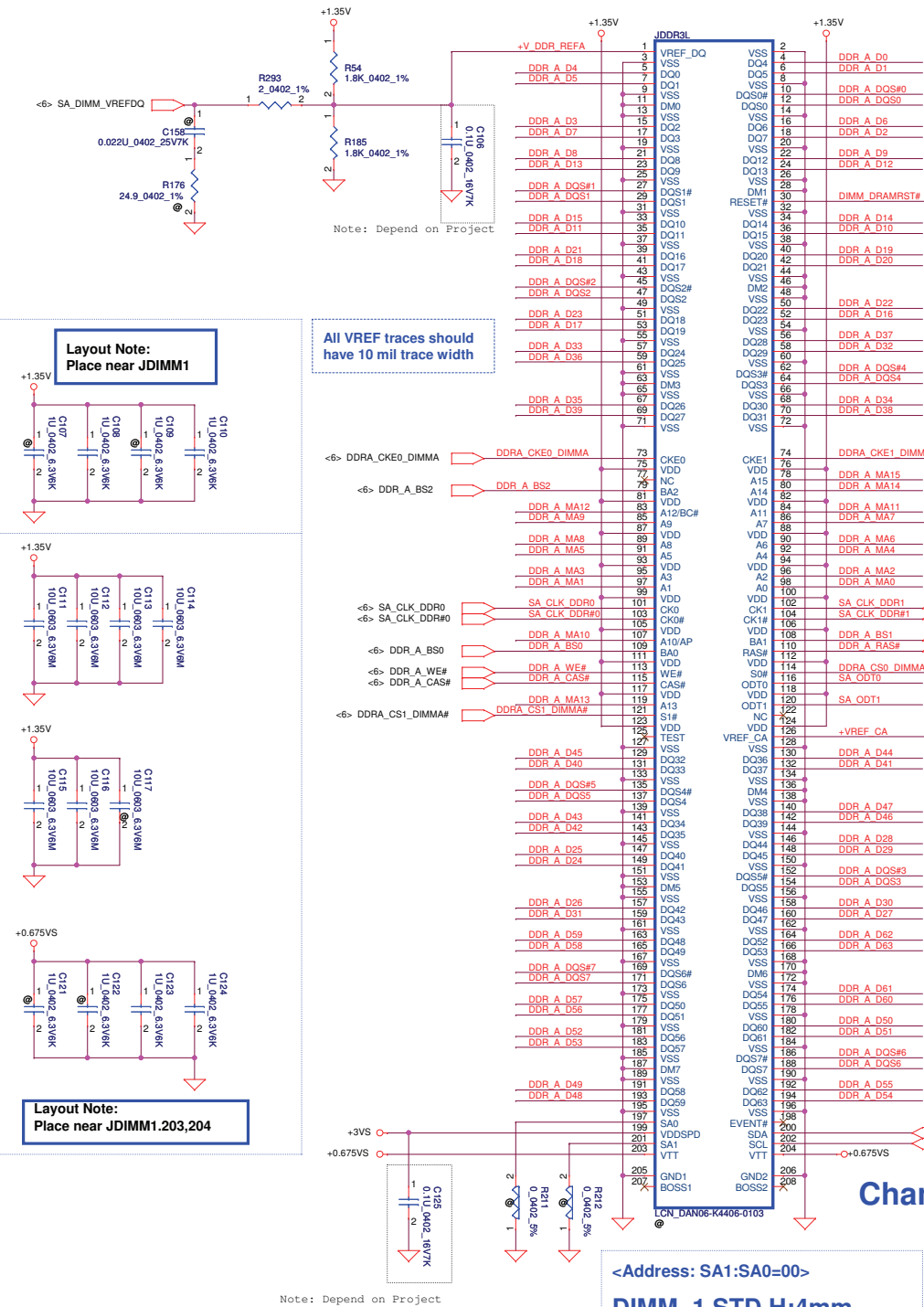


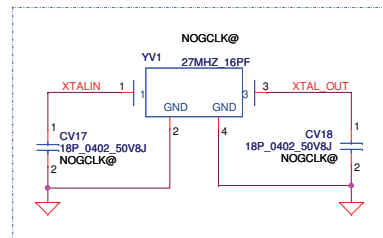
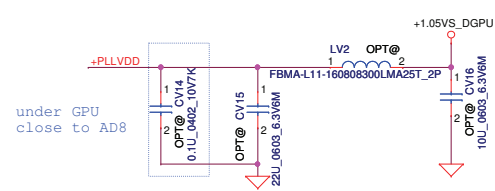
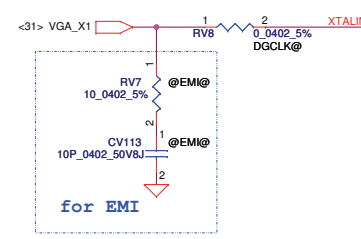
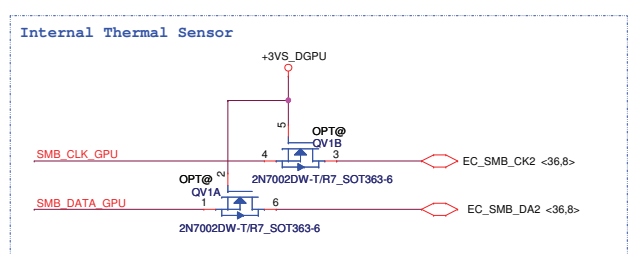
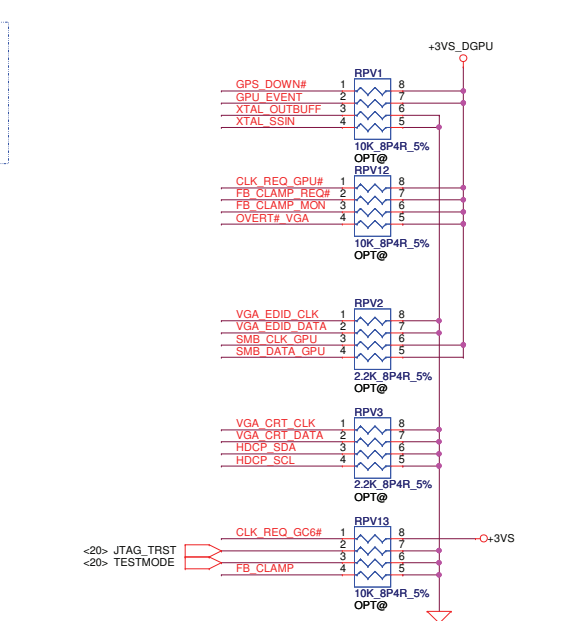
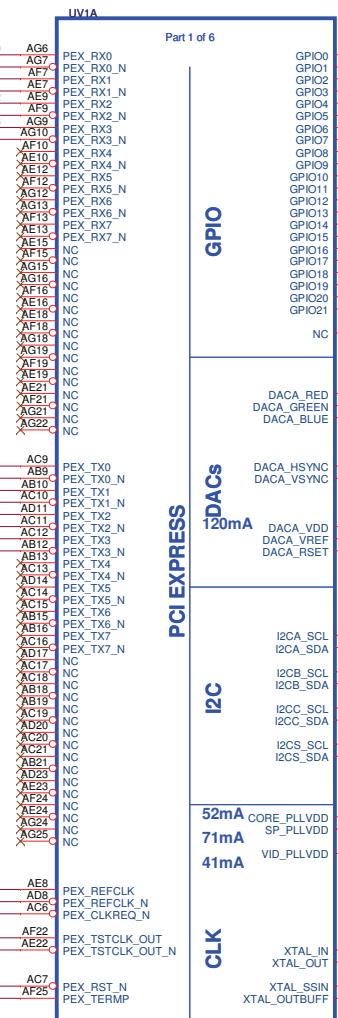
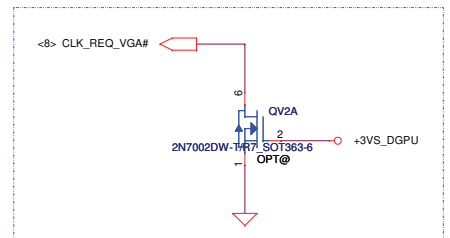
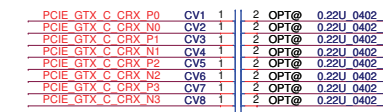
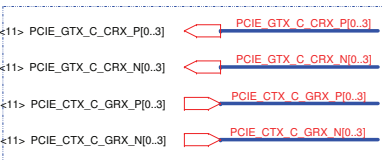
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

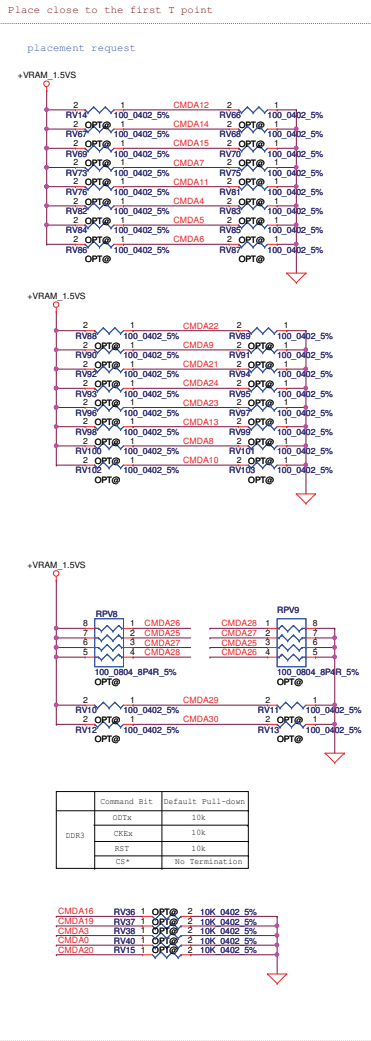
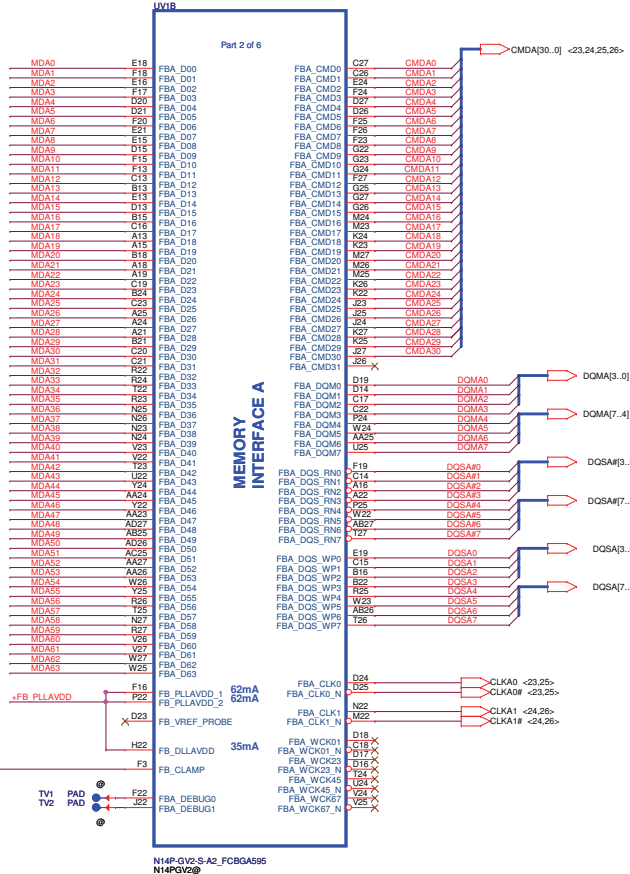
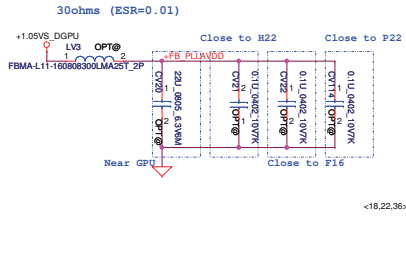
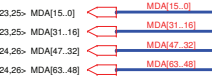
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title
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				Document Number
				ZRMAA/ZEMAA
				Date: Friday, June 21, 2013
				Sheet 15 of 55



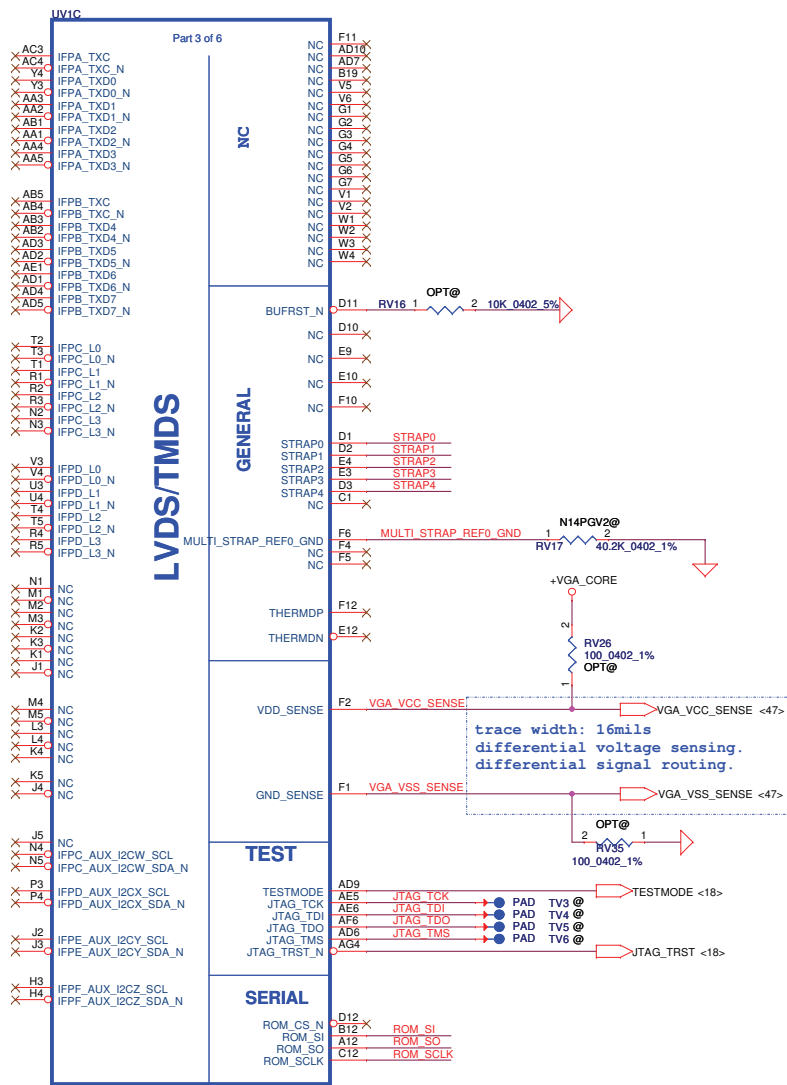


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Issued Date		2012/09/28		Deciphered Date		2013/09/28		Title		VGA N14x PEG & DAC	
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								Document Number	Rev		0.4
C		D		E		Sheet		18 of 55			

VRAM Interface



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		Document Number	Rev 0.4
		Date	Friday, June 21, 2013
		Sheet	19 of 55

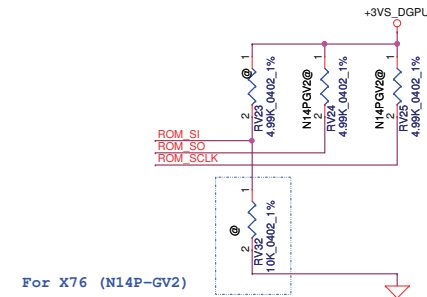
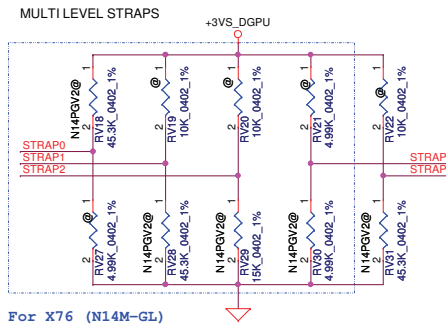


N14P-GV2-S-A2_FCBGA595
N14PGV2@

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

SKU	Device ID	bit5 to bit0
N14P-GV2	TBD	010010
N14M-GL	0x1140	000000

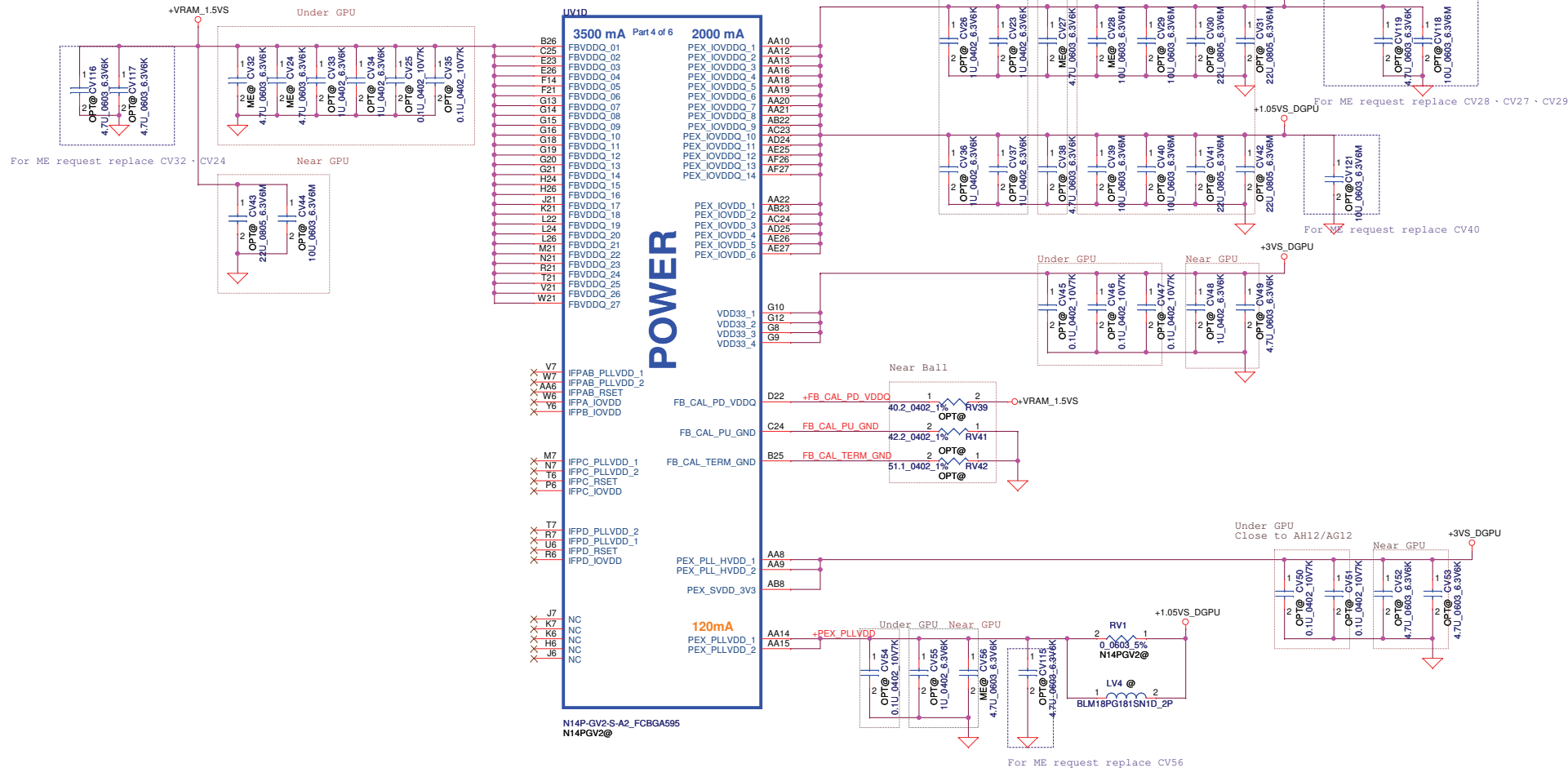
Resistor Values	Pull-up to +3VS_DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



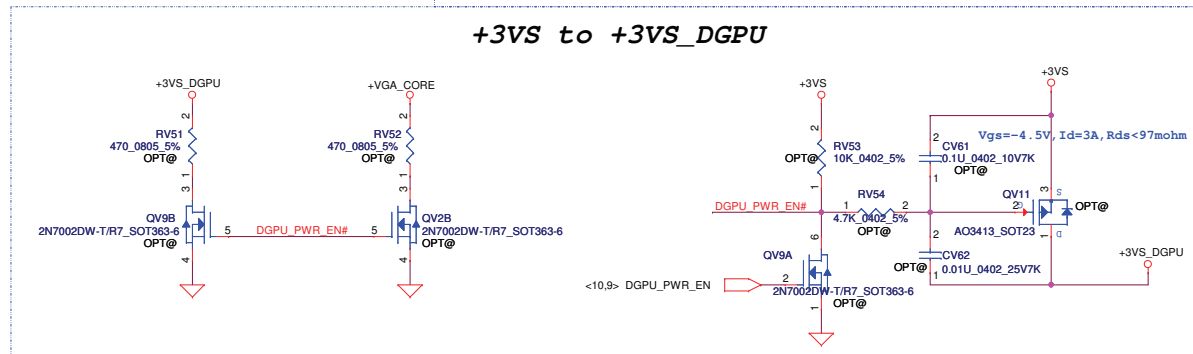
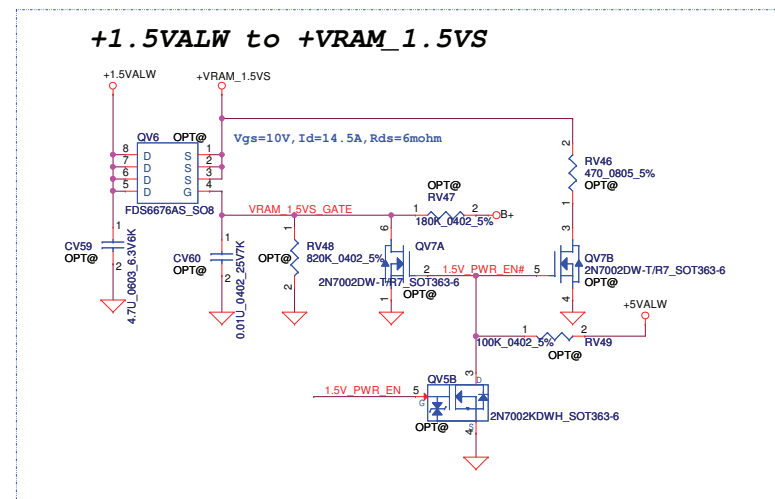
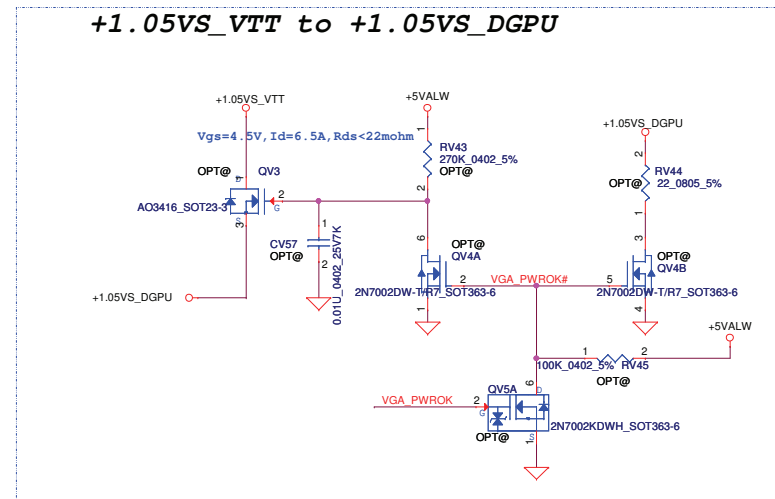
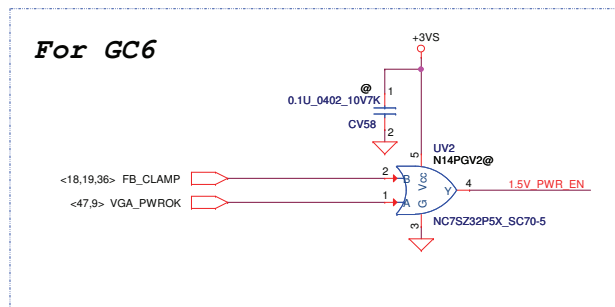
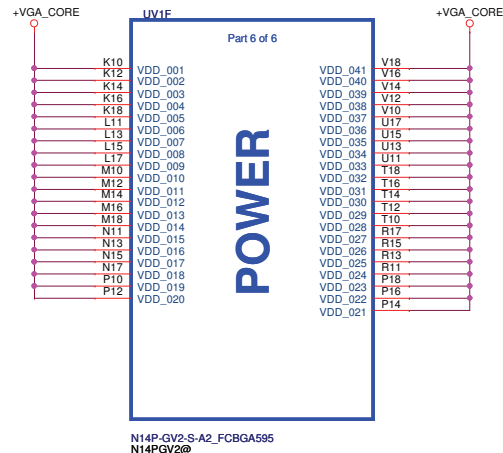
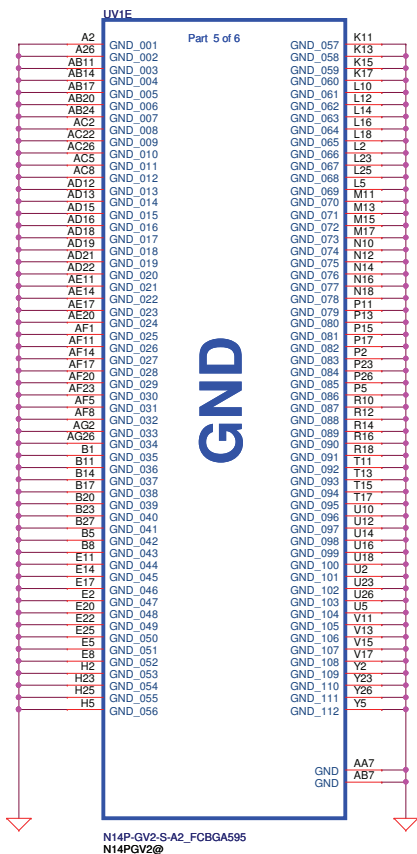
GPU	FB Memory gDDR3	ROM_SI
N14P-GV2	1 Samsung 900MHz K4W2G1646E-BC11	PD 45K
	2 1GHz K4W2G1646E-BC1A	
	8	
	M	
	x 1	
	6 Micron 900MHz MT41K128M16JT-107G	PD 30K
N14M-GL	2 Samsung 900MHz K4W4G1646B-BC11	PD 20K
	5 1GHz K4W4G1646B-BC1A	
	6	
	M	
	x 1	
	6 Micron 900MHz MT41K256M16HA-107G	PD 10K

GPU	FB Memory gDDR3	STRAP[3:0]
N14P-GV2	1 Samsung 900MHz K4W2G1646E-BC11	0101
	2 1GHz K4W2G1646E-BC1A	
	8	
	M	
	x 1	
	6 Hynix 900MHz H5TQ2G63DFR-11C	0110
N14M-GL	2 Hynix 900MHz H5TQ2G63DFR-N0C	
	5	
	6	
	M	
	x 1	
	6 Micron 900MHz MT41K128M16JT-107G	0001
N14M-GL	2 Samsung 900MHz K4W4G1646B-BC11	1011
	5	
	6	
	M	
	x 1	
	6 Hynix 900MHz H5TC4G63AFR-11C	0100
N14M-GL	2 Micron 900MHz MT41K256M16HA-107G	1101
	5	
	6	
	M	
	x 1	
	6	

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				Date: Friday, June 21, 2013	Sheet 20 of 55

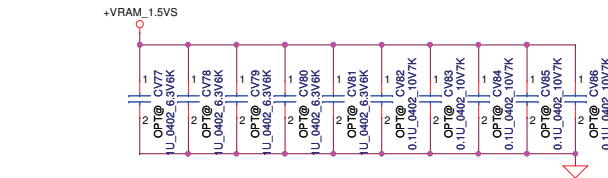
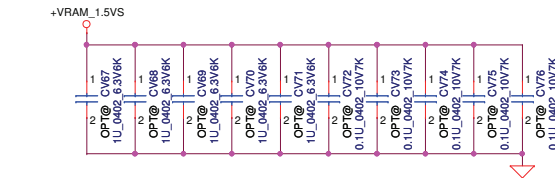


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				Date: Friday, June 21, 2013	Sheet 21 of 55

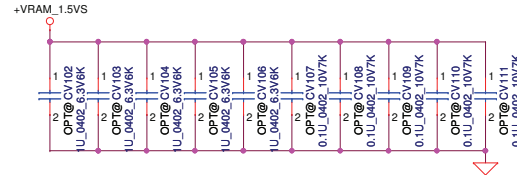
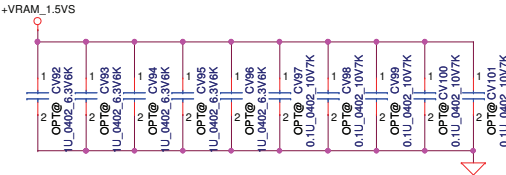


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				Date: Friday, June 21, 2013	Sheet 22 of 55


VRAM DDR3 Chips



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Place close to the first T point



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<19,26> CLKA1#

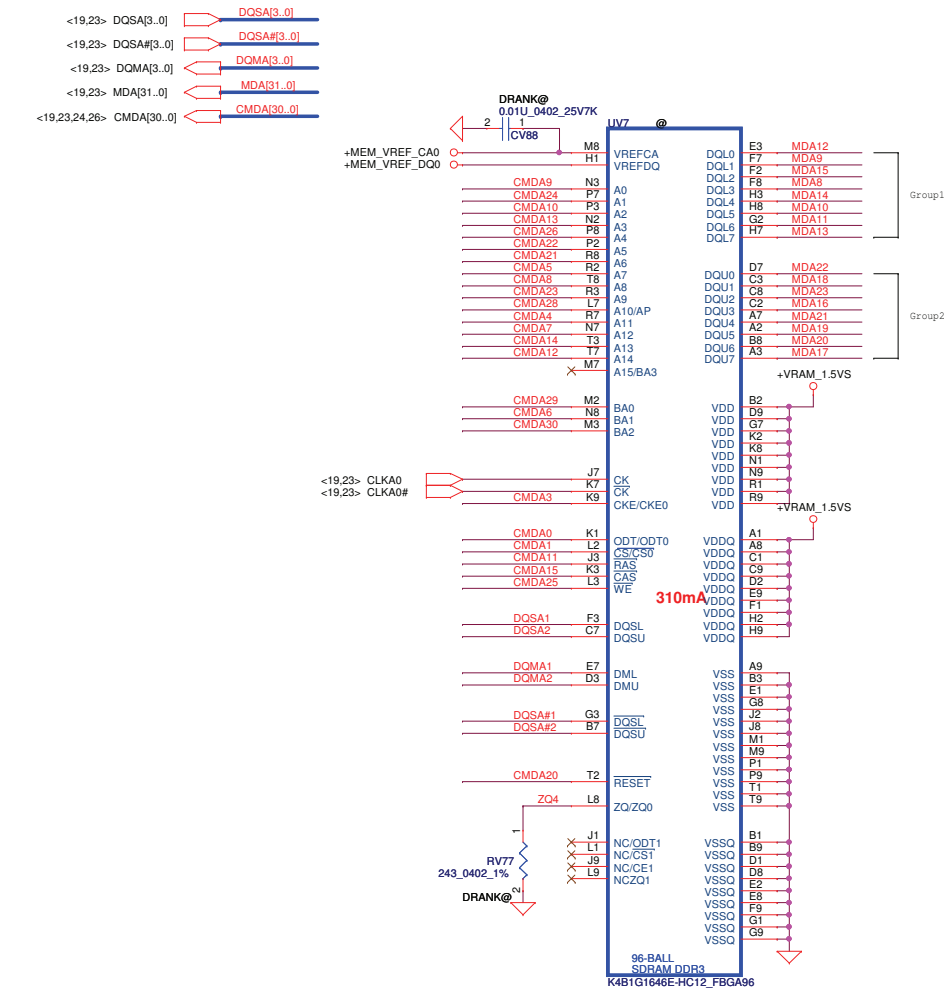
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2

OPT@RV74

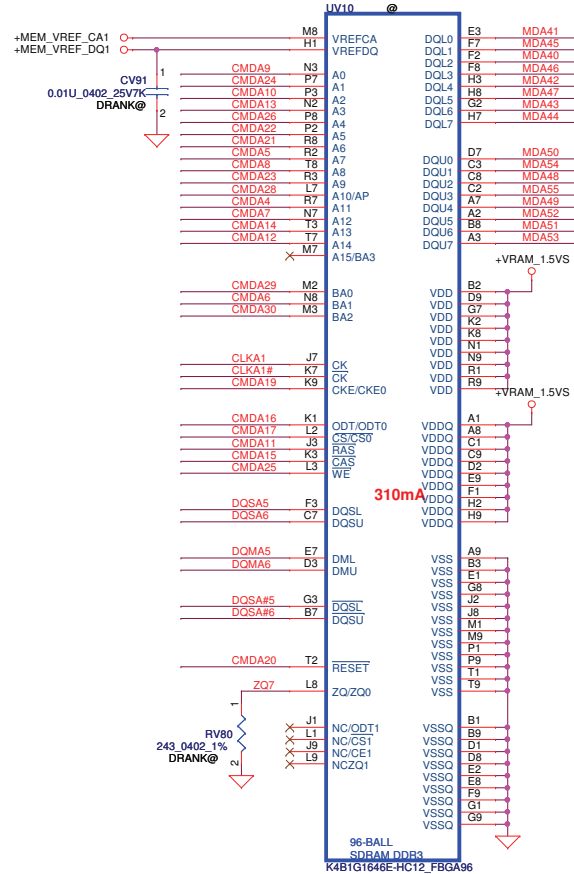
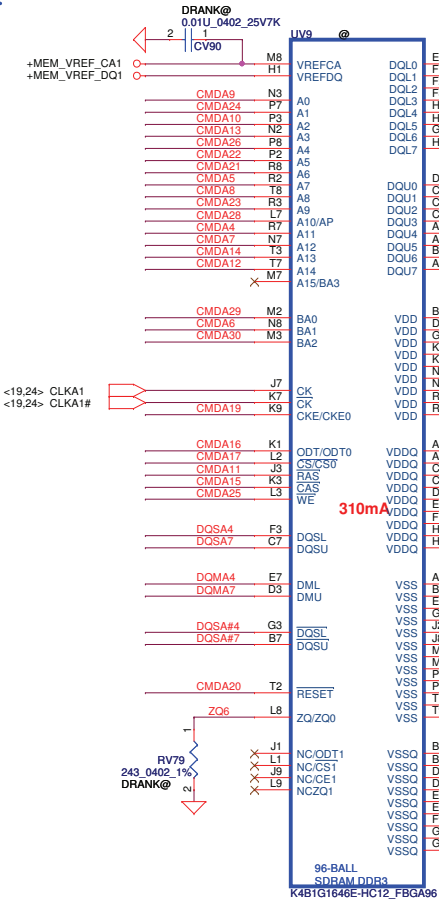
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RANK 1 [31...0]
VRAM DDR3 Chips

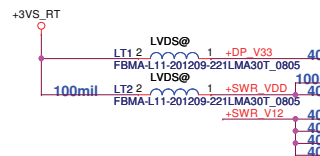
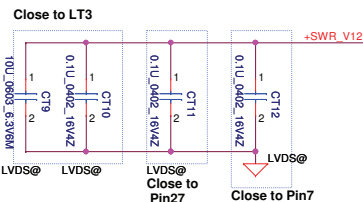
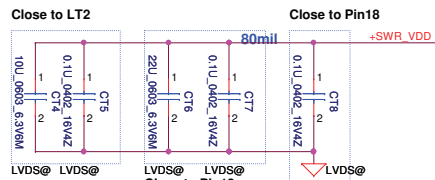
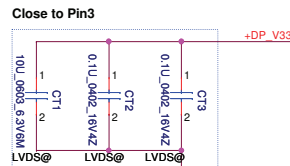


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

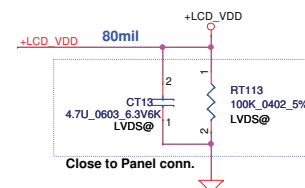
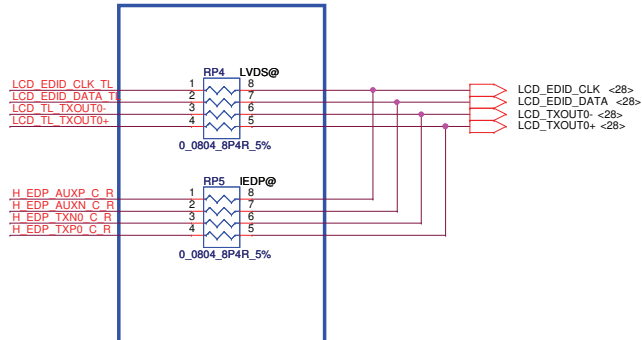
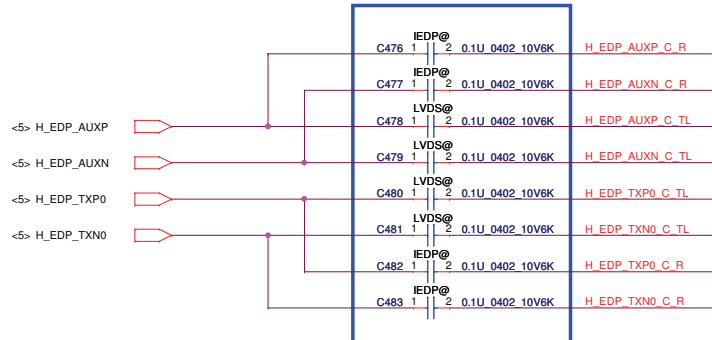
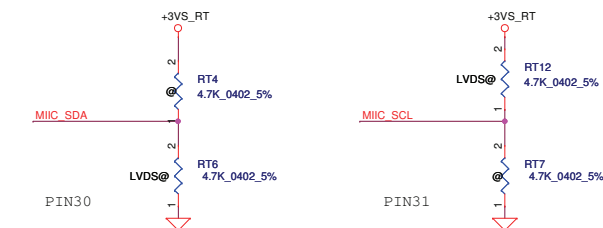
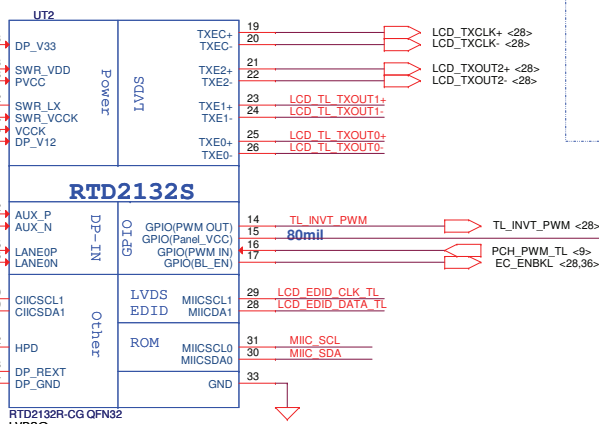
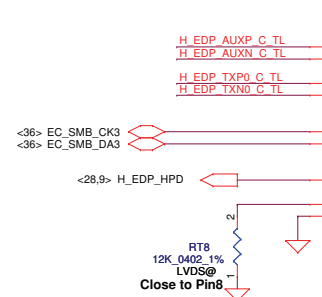
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Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



※LDO mode is adopted as default power regulator mode.
Also can implement SWR mode by add inductor.



	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

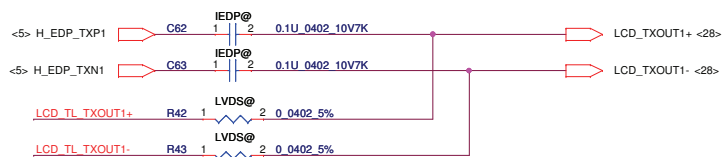
* Version R internal Power Switch, ca output 1A. Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

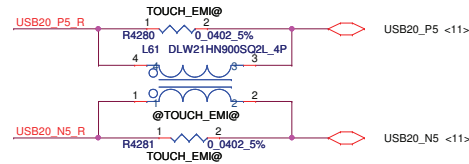
Different between 2132S and 2132R

2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

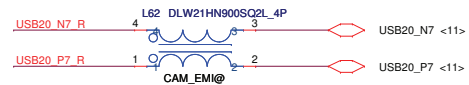


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				Document Number	Rev 0.4	
Date: Friday, June 21, 2013				Sheet	27	of 55

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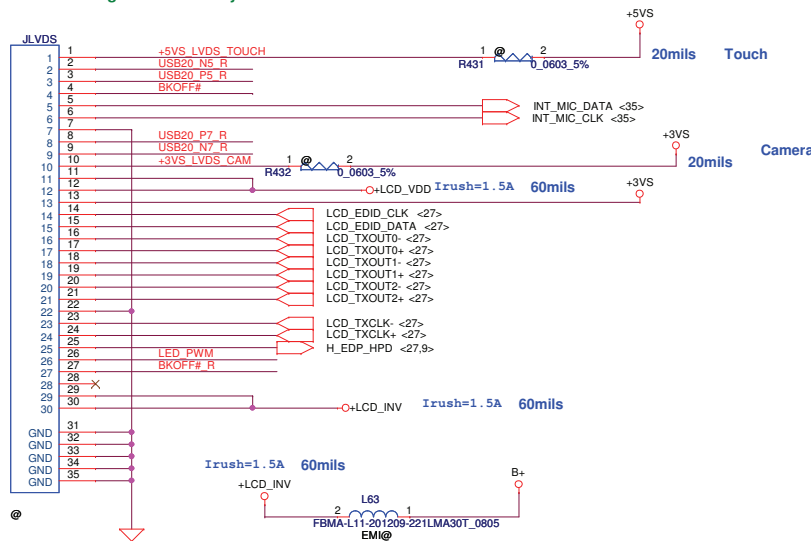


EMI request - Close to JEDP connector

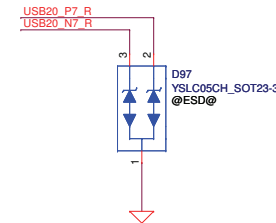
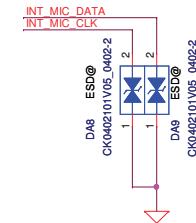
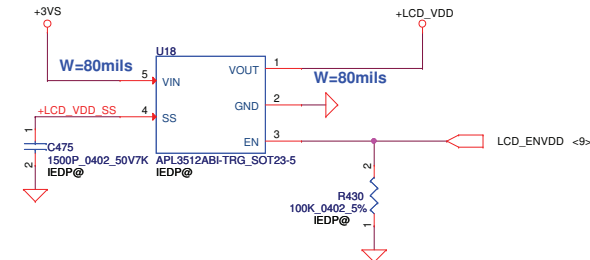


LVDS colay eDP cable

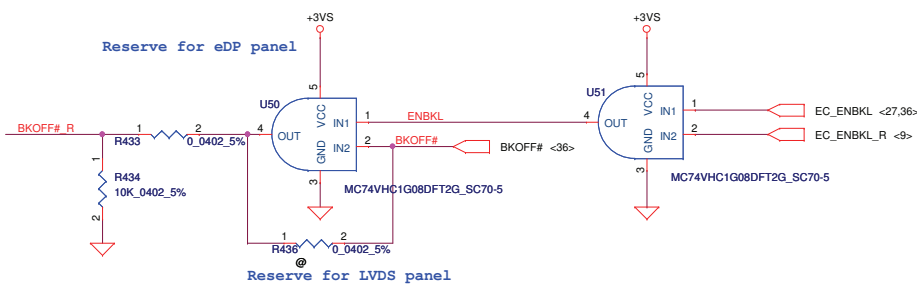
Pin define will be change after ME ready



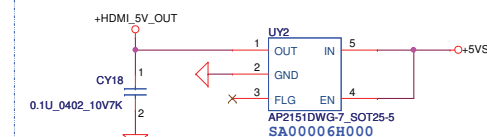
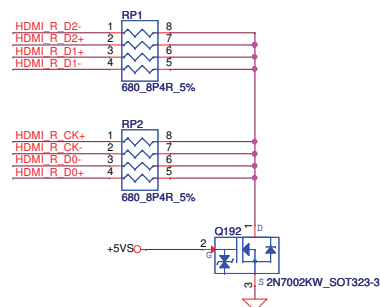
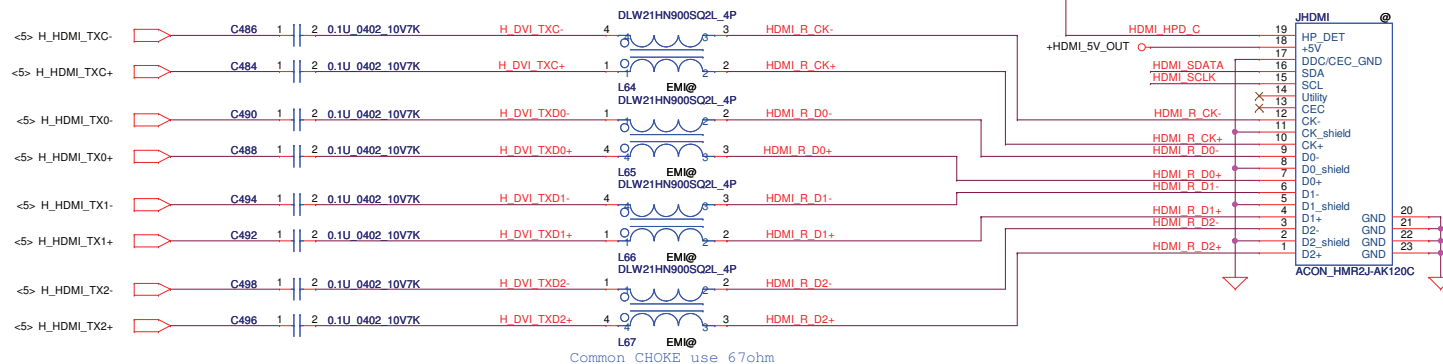
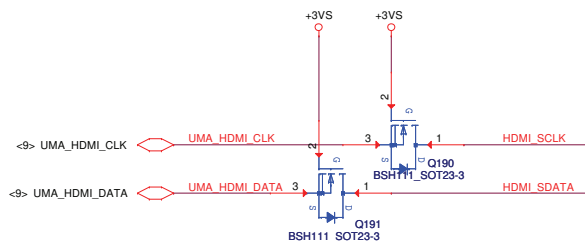
LCD POWER CIRCUIT (For EDP panel only)



Reserve for eDP panel

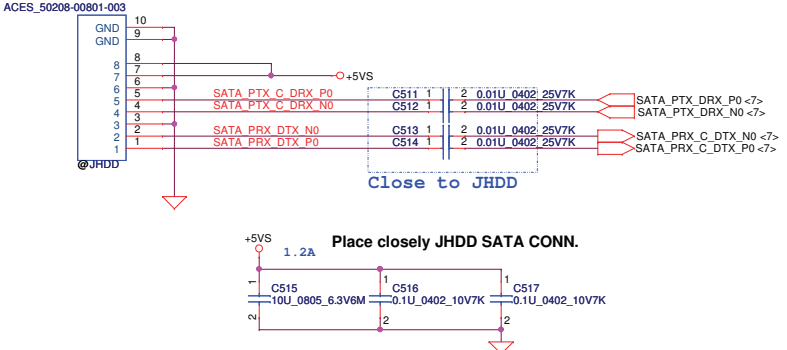


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Issued Date				2012/04/19				Title			
Deciphered Date				2015/04/19				LVDS			
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				Rev				ZRMMA/ZEMAA			
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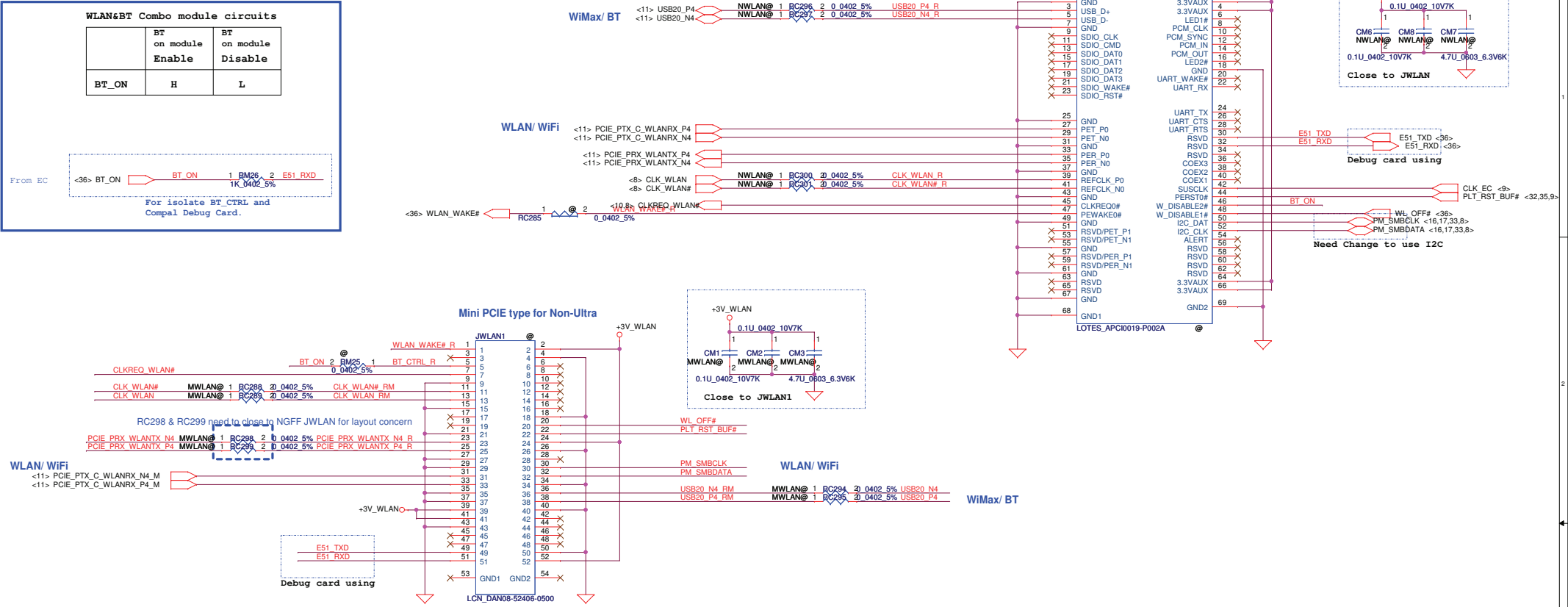
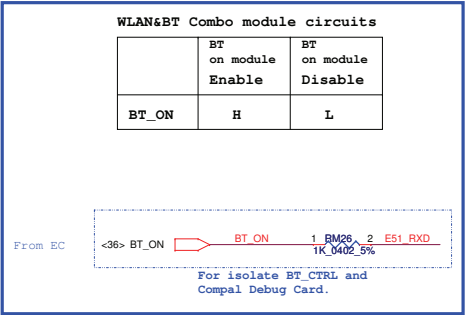


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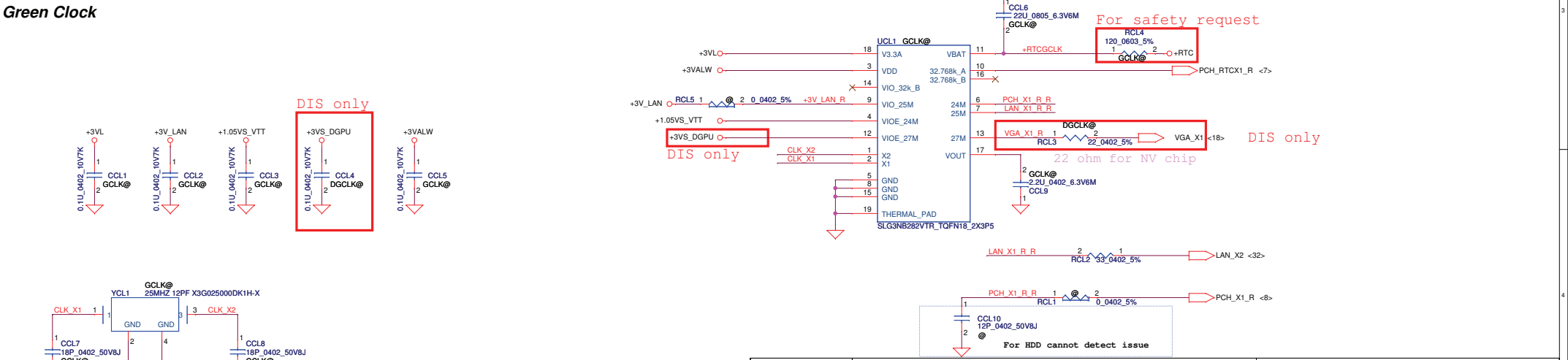
SATA HDD Conn.



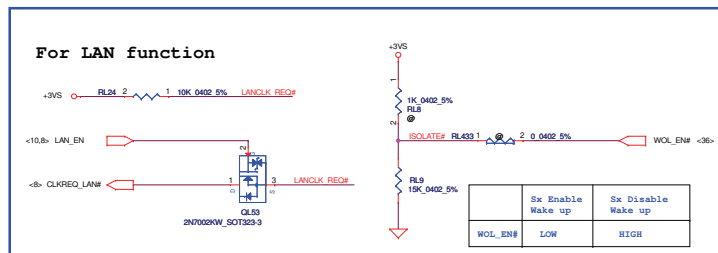
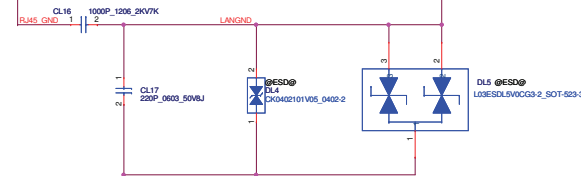
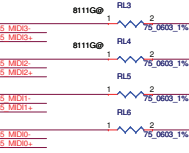
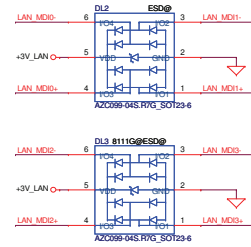
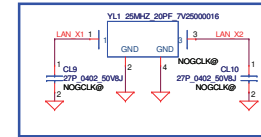
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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	HDD/Gsensor
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Slot 1 Half PCIe Mini Card-WLAN

Green Clock



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Compal Electronics, Inc.

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

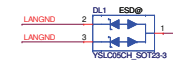
LAN	WOL	LAN_EN		ISOLATED	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

```

★
S3:  after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

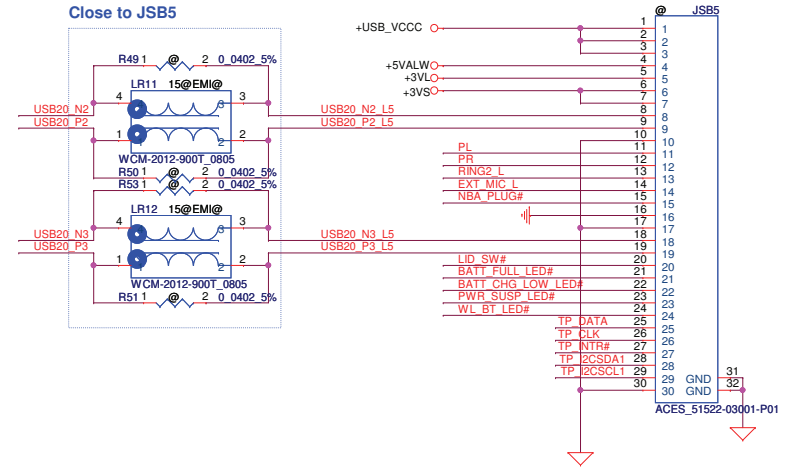
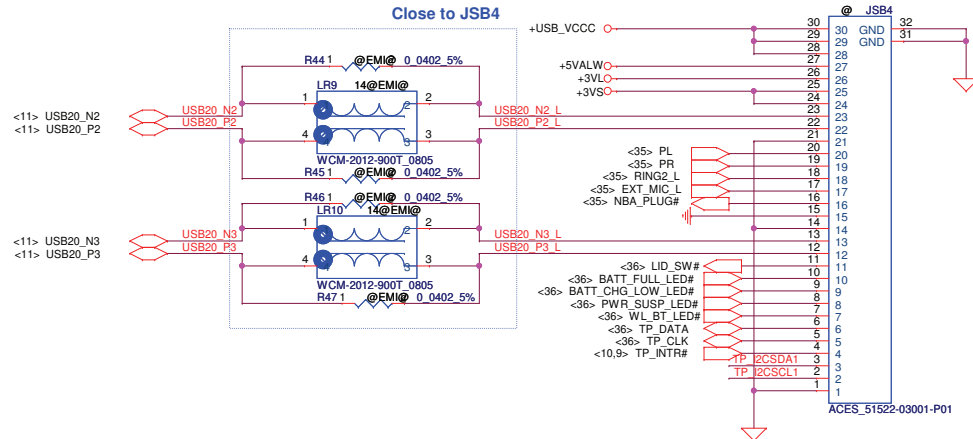
```

For ESD, keep close to RJ45 Connector
Change back to connect to LANGND only
on 20130201

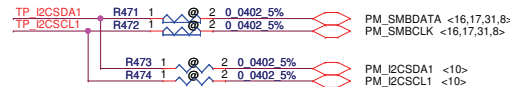
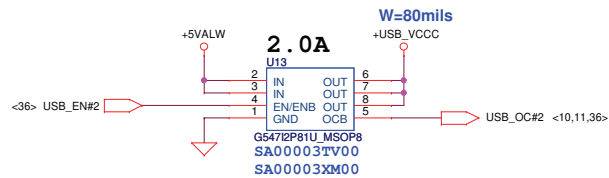


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Small board Conn

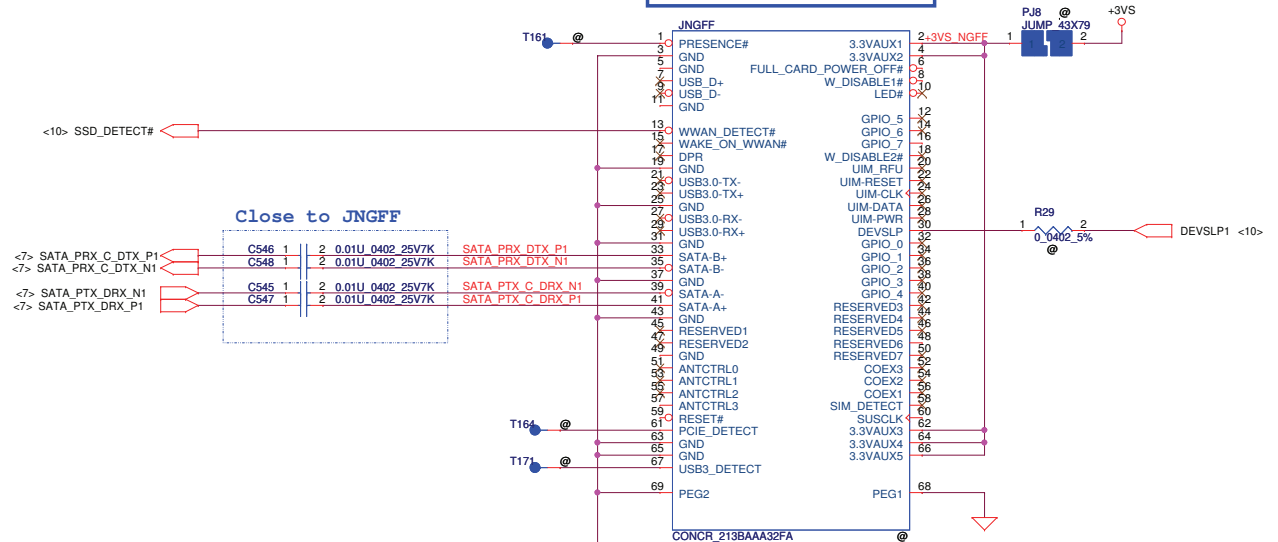


Left USB 2.0 x 1

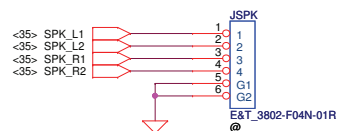


NGFF SSD B Type connector

P/N:SP071212280



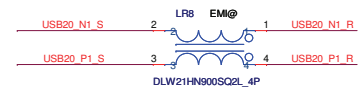
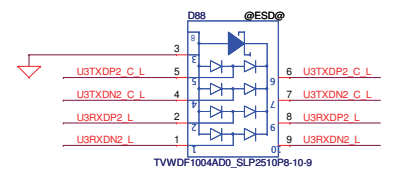
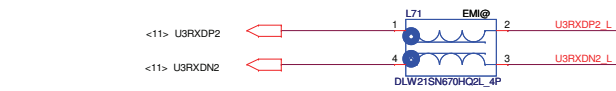
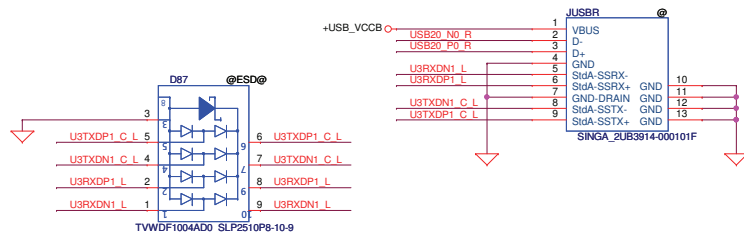
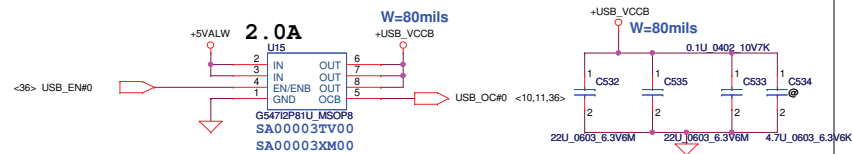
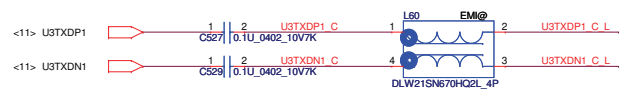
SPK Conn.



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Size Custom	Document Number	ZRMAA/ZEMAA		Rev 0.4
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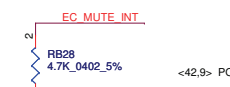
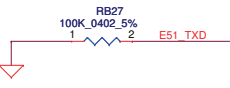
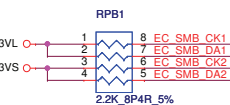
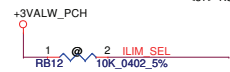
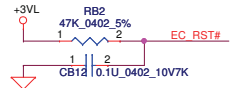
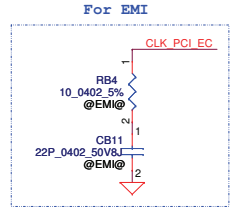
Right side USB 3.0 x 1 W/ Sleep&Charge

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto/Alternate	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

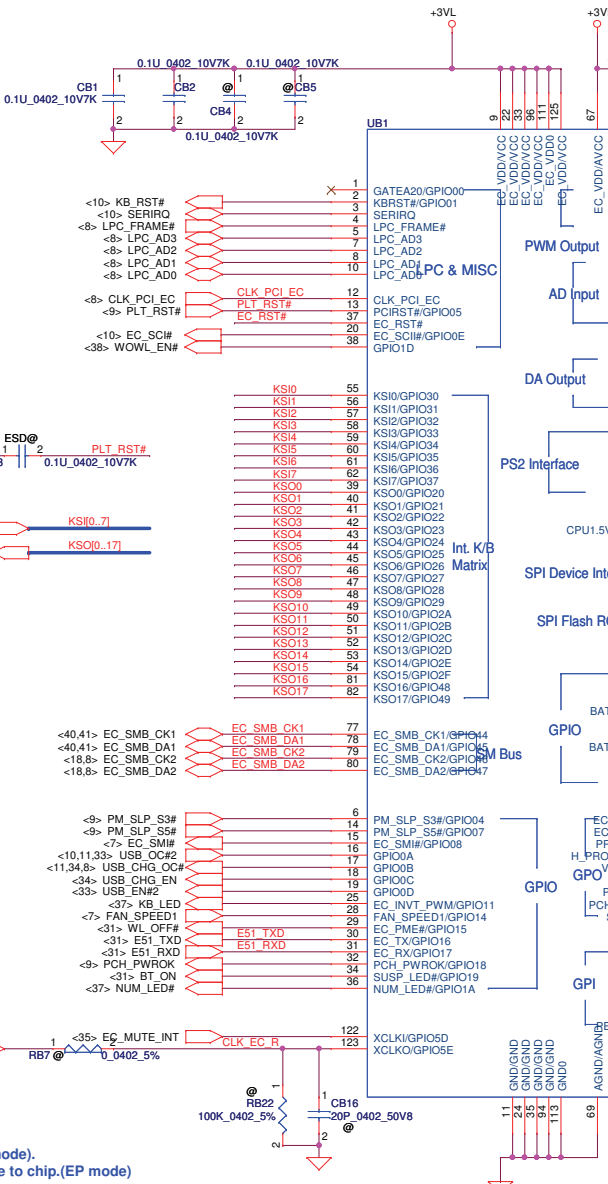
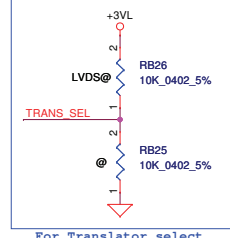


Pin connection diagram for the USB module. The module is labeled **W=100mils** and **SINGA_2UB3914-000101F**. The connections are as follows:

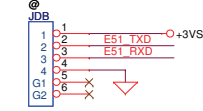
- +USB_VCCA** is connected to pin 1.
- USB20 P1 N** is connected to pin 2.
- USB20 P1 R** is connected to pin 3.
- U3RXDP2 L** is connected to pin 4.
- U3RXDP2 R** is connected to pin 5.
- U3TXDP2 C L** is connected to pin 6.
- U3TXDP2 C R** is connected to pin 7.
- U3TXDP2 C R** is connected to pin 8.
- Pin 10** is connected to GND.
- Pin 11** is connected to GND.
- Pin 12** is connected to GND.
- Pin 13** is connected to GND.



Signal pull high is default status (ROM only mode).
If signal pull low, EC will send translator code to chip.(EP mode)

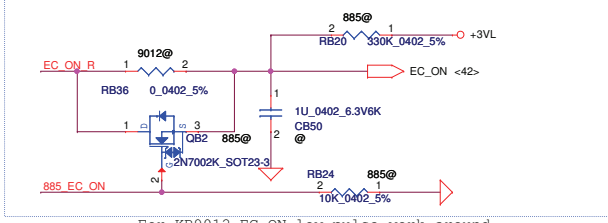
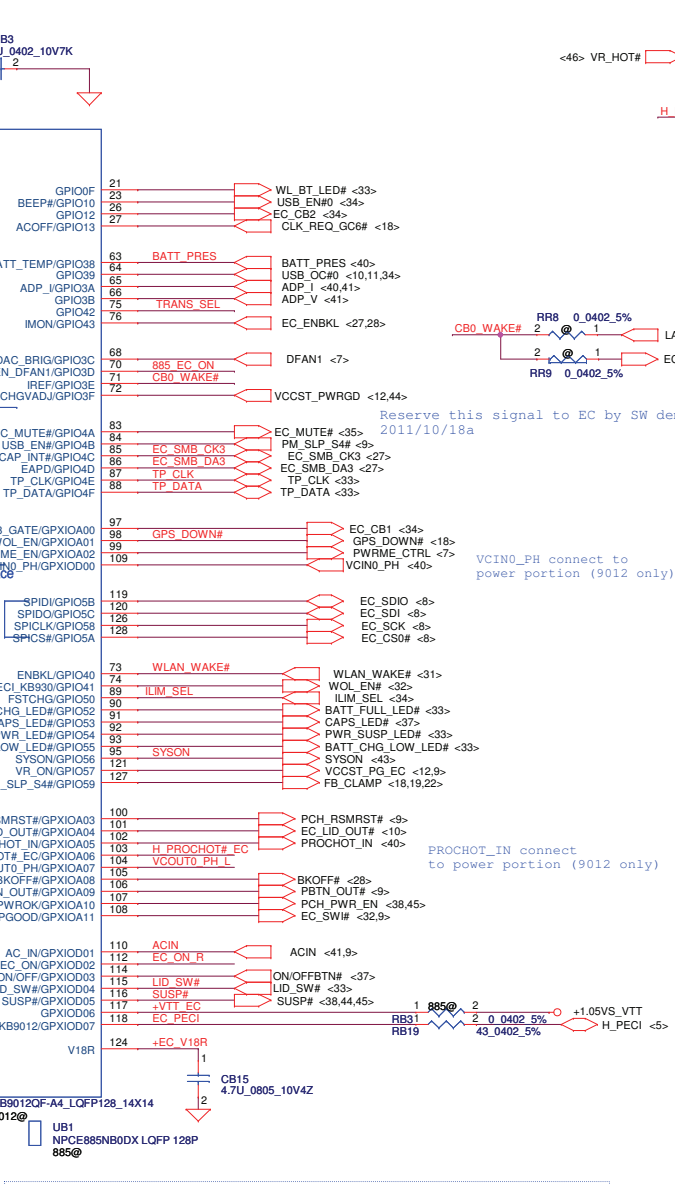


EC DEBUG port

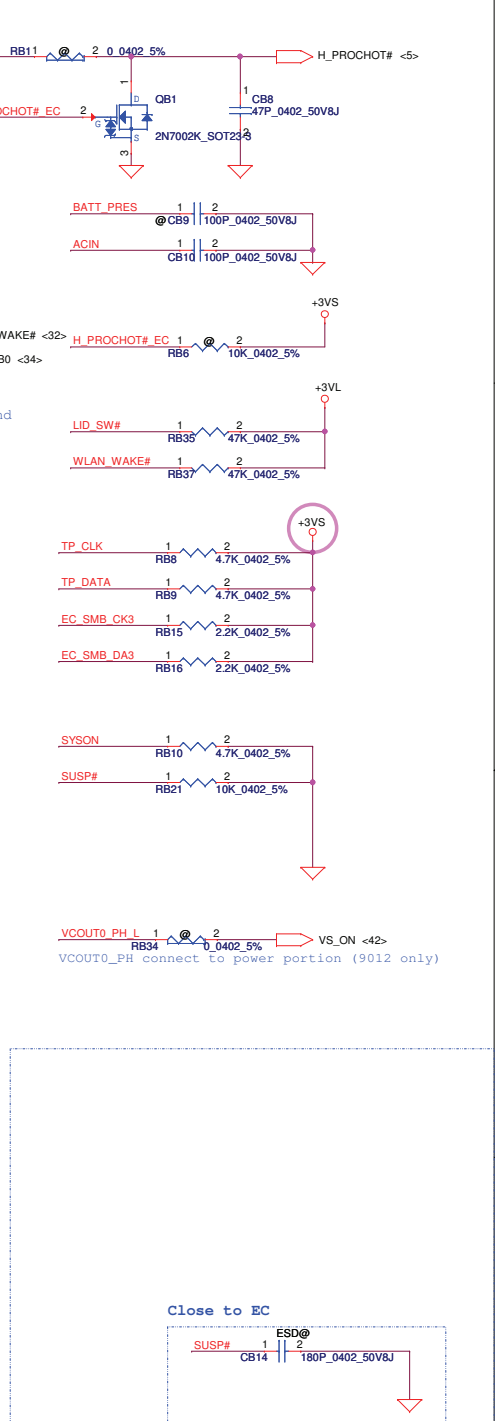


Voltage Comparator Pins FOR 9012 A3

VIN pin	>1.2V	<1.2V
VIN1 pin109	HIGH	LOW
VIN1 pin102	HIGH	LOW
VOUT0 pin104	HIGH	LOW
VOUT1 pin103	HIGH	LOW



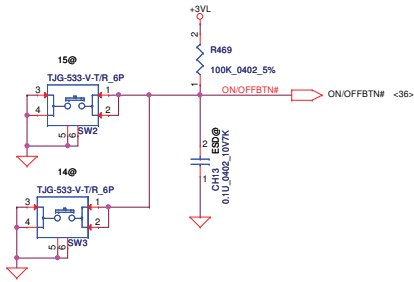
For KB9012 EC_ON low pulse work around



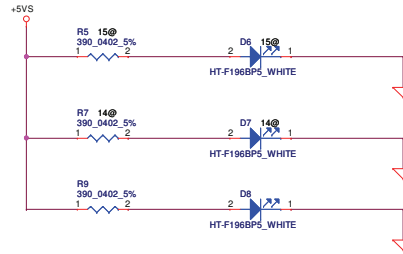
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LPC-EC-KB9012&930	
Title	Document Number
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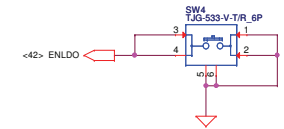
Power Button



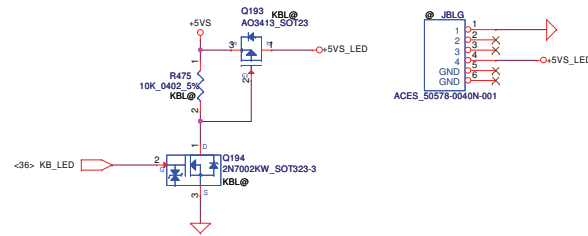
POWER LED



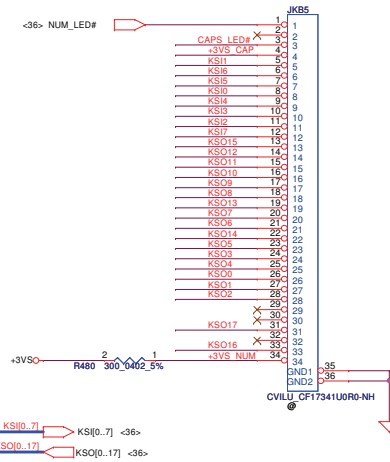
Battery Reset



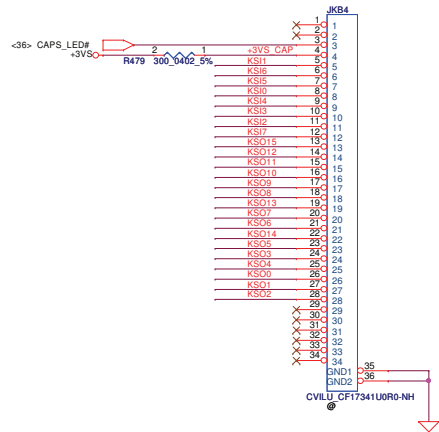
Keyboard LED



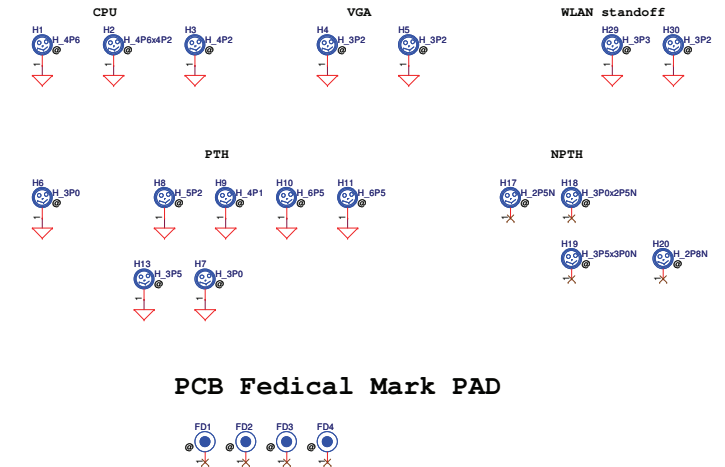
15 " KEYBOARD CONN.



14 " KEYBOARD CONN.



Screw Hole



PCB Federal Mark PAD

ISPD

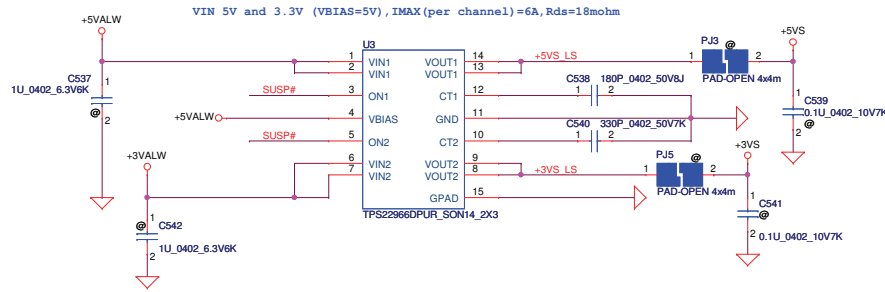


GPU

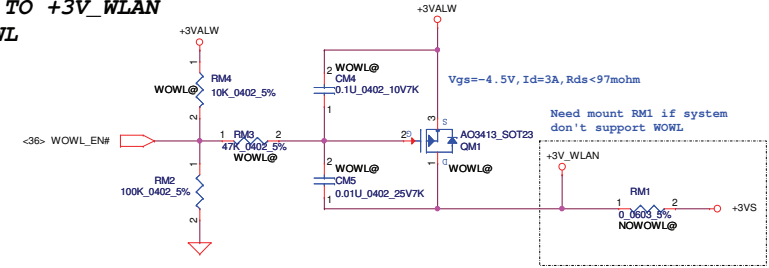


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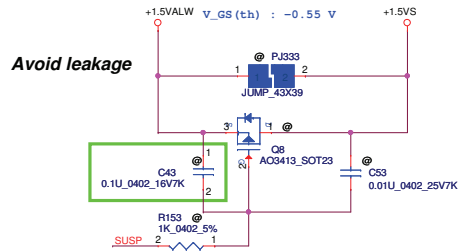
+3VALW TO +3VS **+5VALW TO +5VS** **Load Switch**

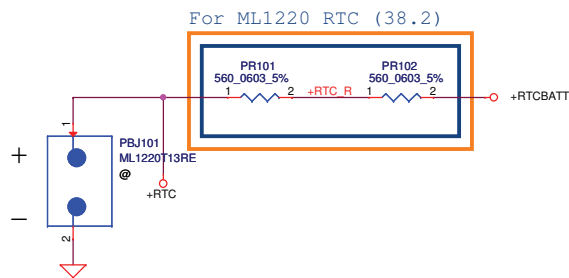
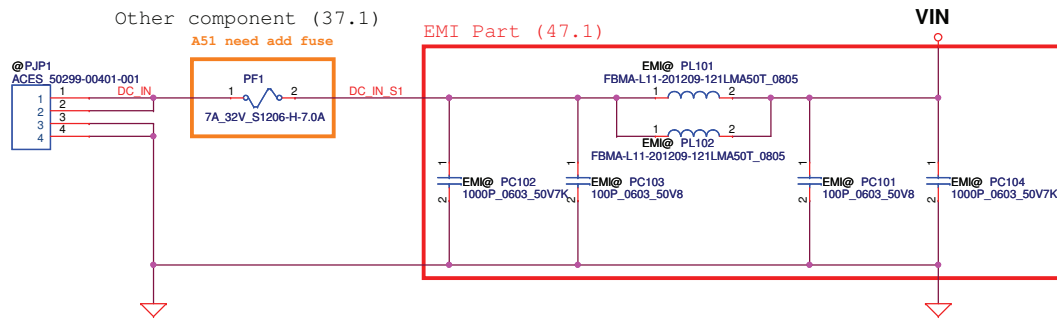


+3VALW TO +3V_WLAN **for WOWL**

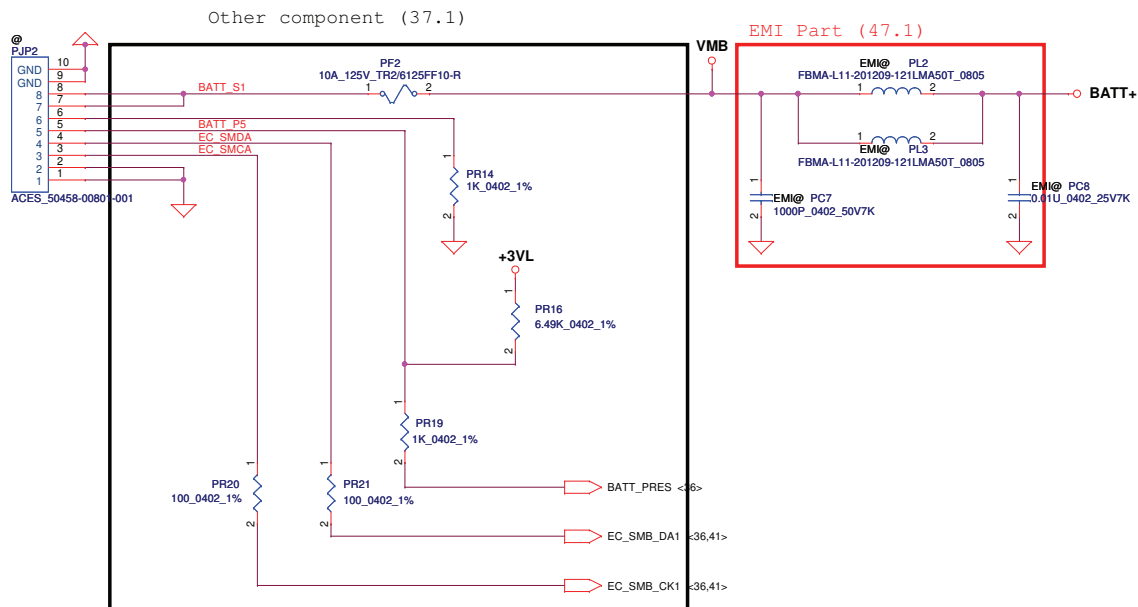


+1.5VALW to +1.5VS

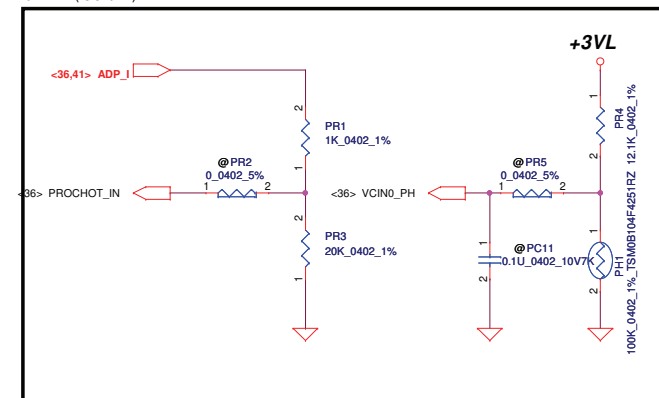




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OTP (39.7)

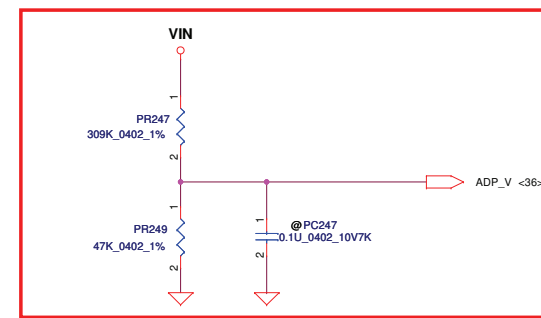


	Initial	Recovery
45W UMA	0.55V	0.43V
75W N14P-GV2	0.90V	0.72V

	Initial	Recovery
CPU OTP	90 C	70 C

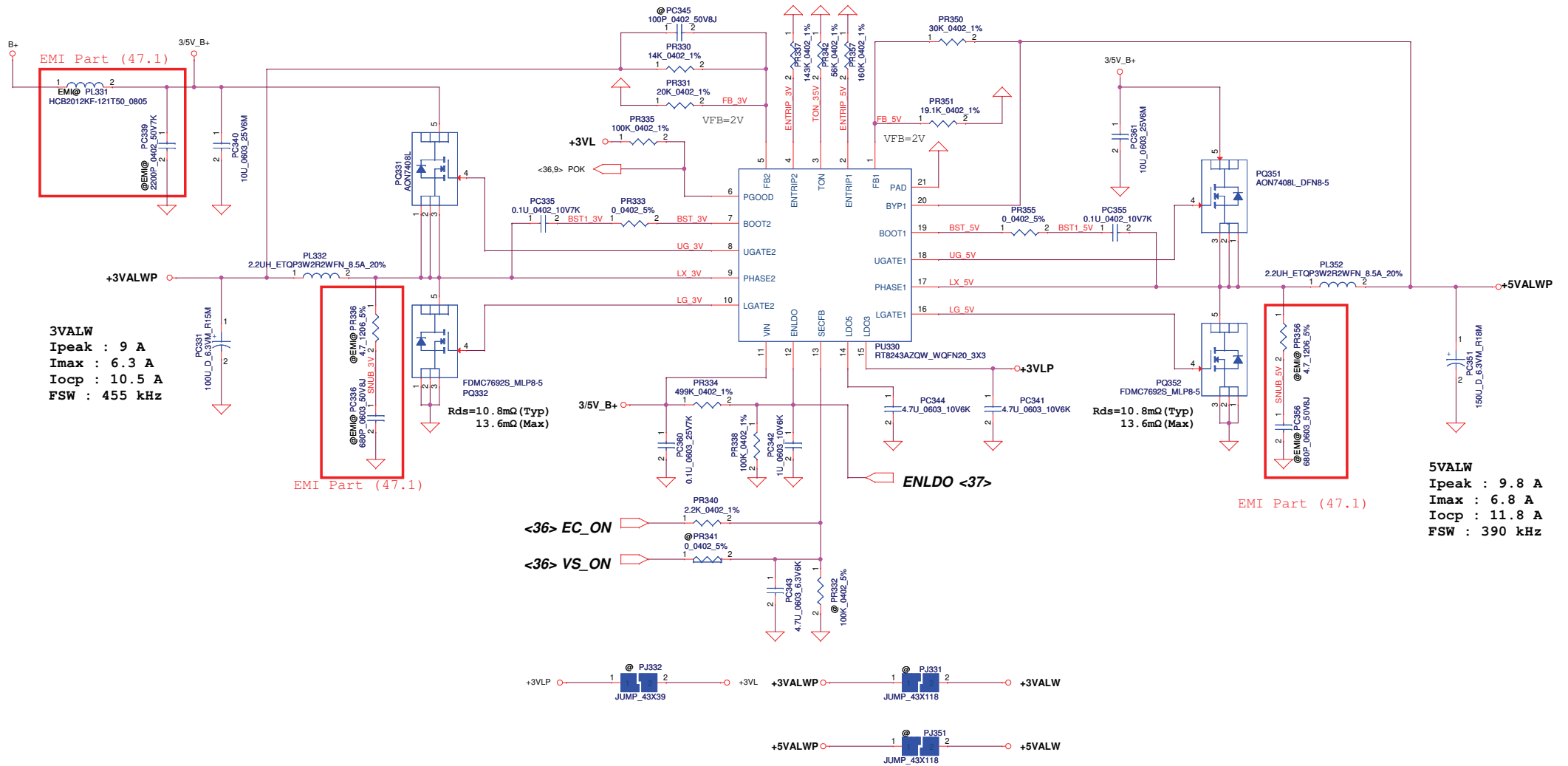
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Issued Date		Deciphered Date		Title	BATTERY CONN / OTP
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Charger controller (40.1), Support component (40.2)

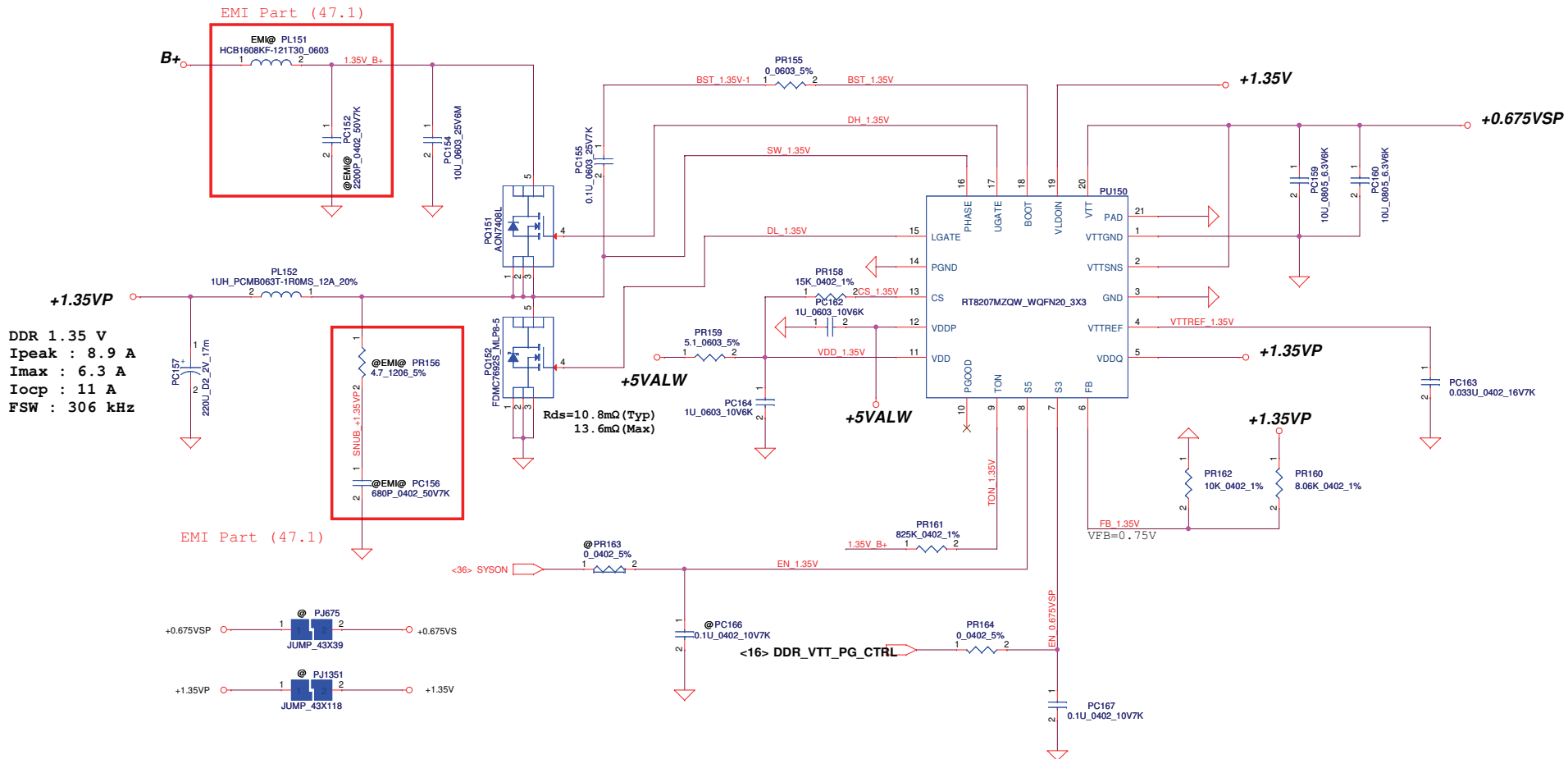


Vin Dectector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
3.61A			

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						Size		Document Number		Rev	
						ZRMAA				0.4	
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DDR controller (35.3), Support component (35.4)



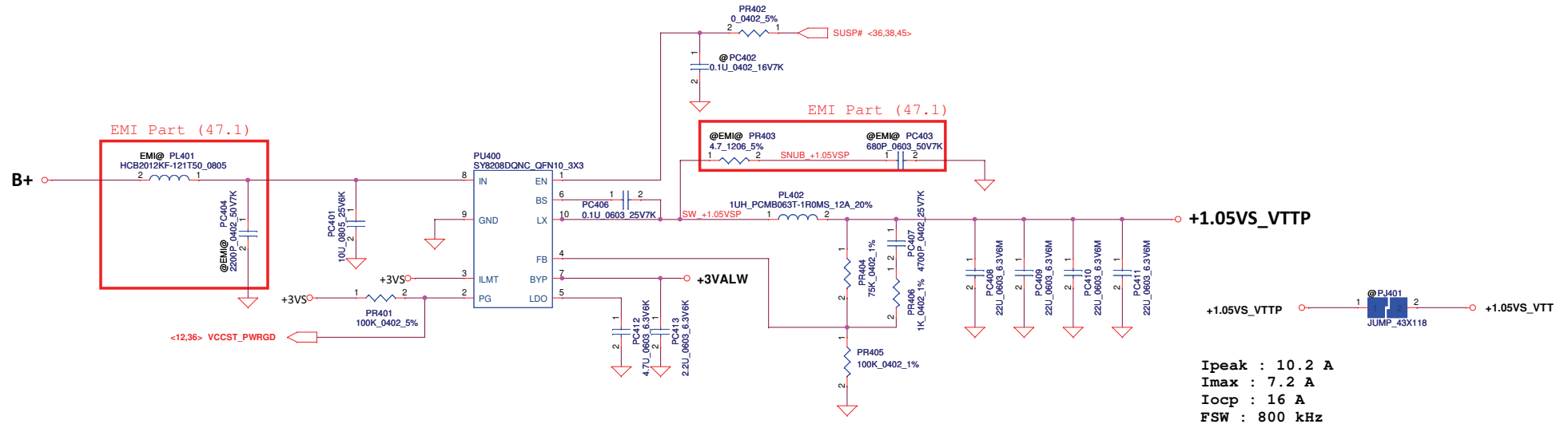
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

WWW.AliSaler.Com

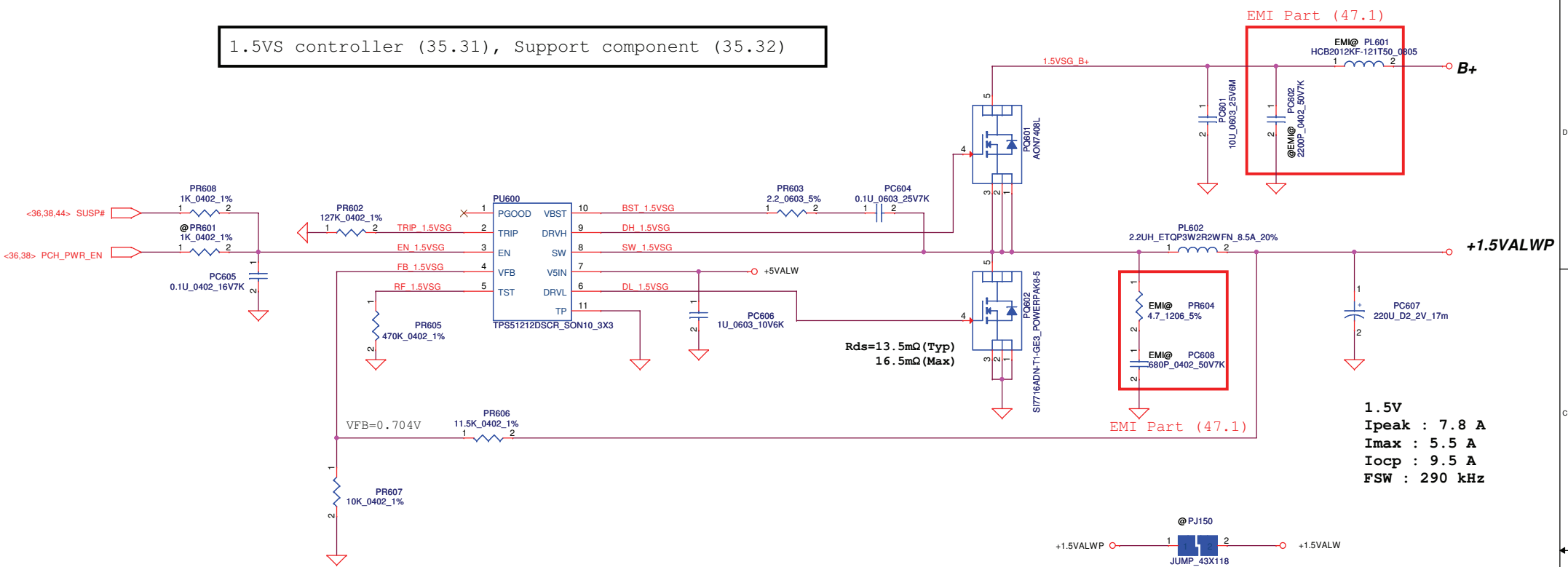
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		Deciphered Date		Title 1.35VP/0.675VSP			
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1.05VCCP controller (35.5), Support component (35.6)



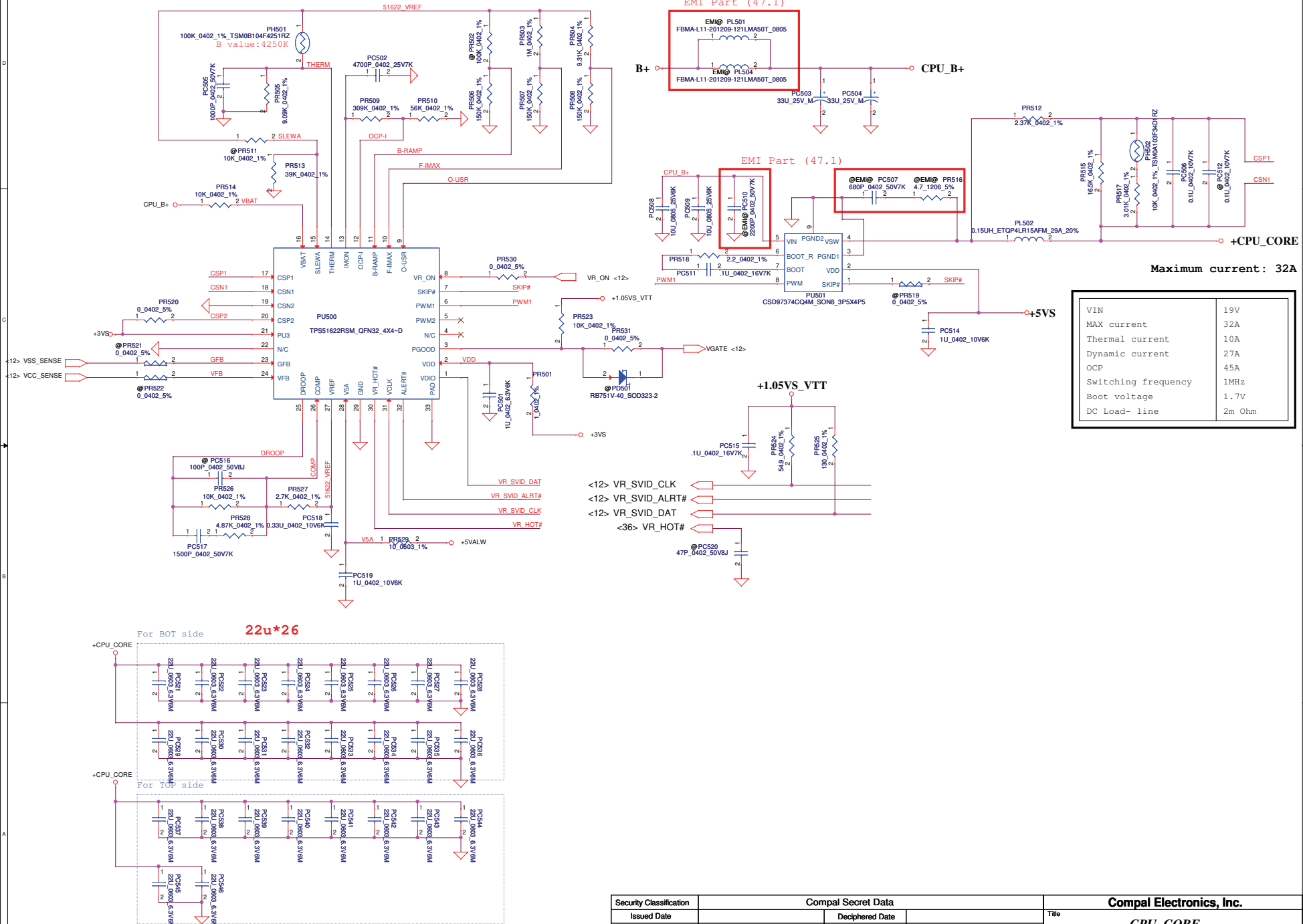
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Title			+1.05VS_VCCP	
Document Number			ZRMMA	
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1.5VS controller (35.31), Support component (35.32)



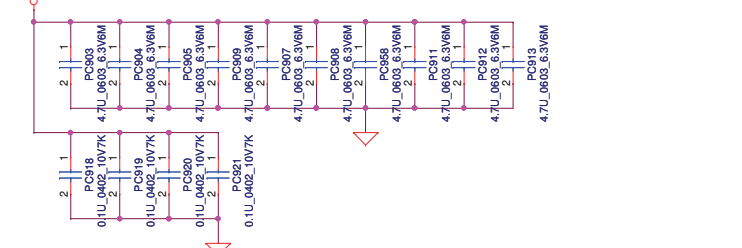
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Issued Date		Deciphered Date		Title +1.5VS		
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+VCC_CORE controller (36.1), Support component (36.3)
driver(36.2), decoupling cap(36.4)

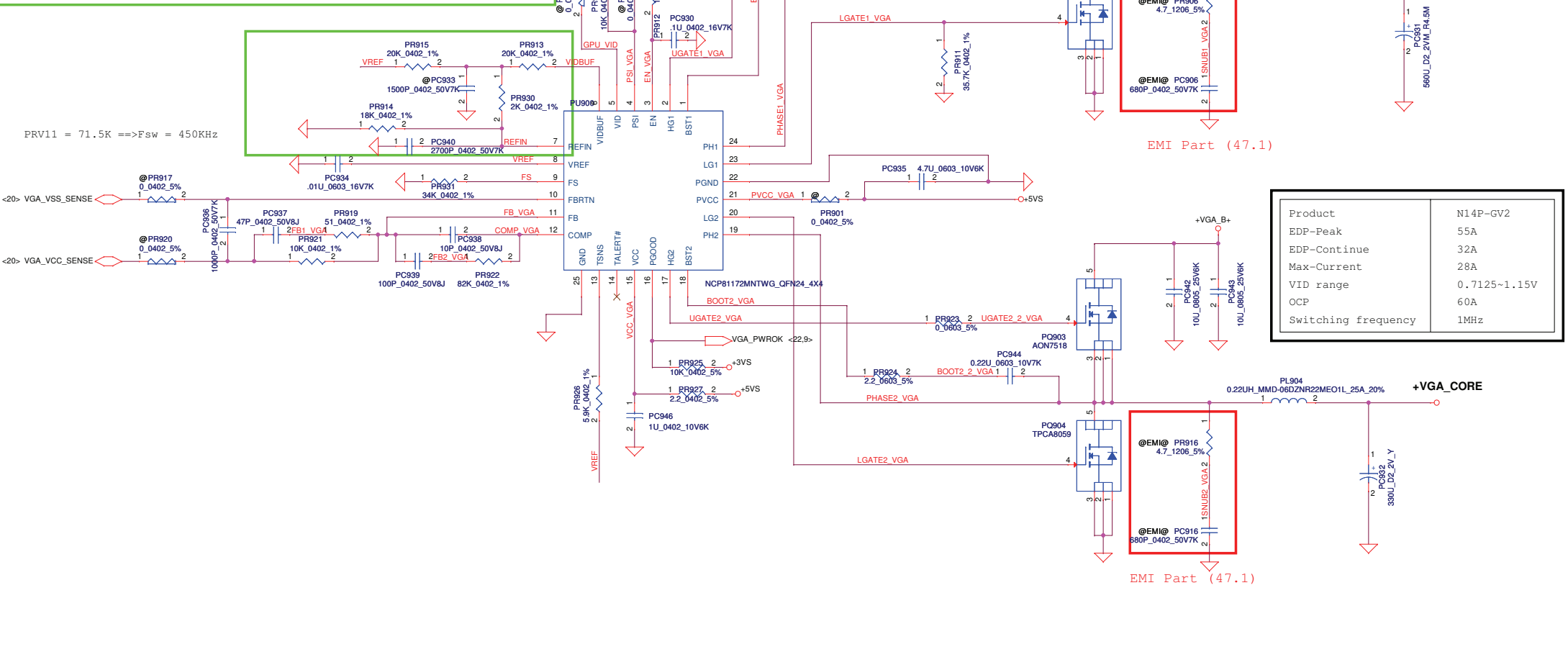
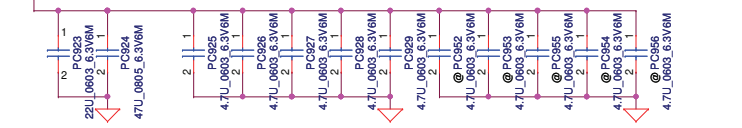


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						ZRMMA		
Date:			Sheet			46 of 55		

+VGA_CORE Under VGA Core GB4-128 package



+VGA_CORE Near VGA Core



Product	N14P-GV2
EDP-Peak	55A
EDP-Continue	32A
Max-Current	28A
VID range	0.7125~1.15V
OCV	60A
Switching frequency	1MHz

Security Classification	Compal Secret Data	Compal Electronics, Inc.	
Issued Date	Deciphered Date	Title	VGA_CORE
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		Rev	0.4
		Sheet	47 of 55

Item	Time (When)	Page (Where)	Location / Discription (How / What)	Request (Who)
1	EVT-2013/04/09	P47-PWR-GPU_CORE	PC930 / Change to Un-pop	HW
2	DVT-2013/04/18	P43-PWR-1.35VP/0.675VSP	PC157 / Change to Polymer CAP (220uF/2V/17m/D2)	Power
3	DVT-2013/04/18	P45-PWR-1.5VALW	PC607 / Change to Polymer CAP (220uF/2V/17m/D2)	Power
4				
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				PIR (PWR)		
				Document Number		
				ZRMAA		
				Rev		
				0.4		
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HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.0 TO 0.1

GERBER-OUT DATE: 2013/04/01

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	03/04	36	Add EC_SMB_CK3、EC_SMB_DA3、RB135、RB136	Vendor request for LVDS Translator
2	03/04	27	Add EC_SMB_CK3、EC_SMB_DA3	Vendor request for LVDS Translator
3	03/04	31	Change JWLAN connector	For WLAN
4	03/04	31	Change JHDMI connector	For HDMI
5	03/04b	30	Change JHDD pin define	For HDD
6	03/04b	33	Delete DEVSLP0	For HDD
7	03/04b	37	ADD R5、D6、R7、D7	For Power LED
8	03/05A	07	Change FAN connector	For FAN
9	03/05A	16、17	Change DDR net order	For DDR
10	03/05A	33	Change JHP connector	For Small board
11	03/05B	19	Change RV4、RV5、RV6、RV7、RV8、RV9	For Layout placement
12	03/06A	19	Delete RV108、RV109、RV110、RV111、RV104、RV105、RV106、RV107	For Layout placement
13	03/06A	19	ADD RPV8、RPV9	For Layout placement
14	03/06A	06	Update DDR pin for DDR interleave routing	For DDR
15	03/06B	33	Change JHP to JSB4 and Add JSB5	For Small board
16	03/06B	33	ADD R44、R45、R46、R47	For Small board
17	03/06B	33	Change JKB to JKB4、ADD JKB5	For Keyboard
18	03/07A	16、17	Change JDDR3S、JDDR3R	For DDR
19	03/11A	33	Change JNGFF connector	For NGFF SSD
20	03/11A	34	Change JUSBR、JUSBF connector	For NGFF SSD
21	03/11A	37	Modify Hole	For Dummy
22	03/11B	35	ADD RA5、Q5539B for Combo Jack Normal Close	For Audio
23	03/11B	07	Change JSPK	For Speaker
24	03/12A	30	Swap JHDD pin define	For HDD
25	03/12A	29	Swap L64、L65、L66、L67	For HDMI
26	03/12A	37	Change D6、D7 material and Add D8、R19	For 14" 15" LED
27	03/12A	37	Add SW3 for 14"	For Power Button
28	03/12B	37	Add H18、H19 Delete H7、H14、H15	For Hole
29	03/12C	37	Change CCL2 and RCL5 @ to GCLK@	For Green clock
30	03/12C	37	Delete E51_TXD(RB27)、E51_RXD	For WLAN
31	03/12D	31	Change JWLAN to NGFF E type	For WLAN
32	03/13A	37	ADD KSO17、KSO16 for 15" keyboard	For keyboard
33	03/13A	36	Change TRANS_SEL to pin75、CHG_PWR_GATE# to pin89	For keyboard
34	03/13A	36	ADD KSO17、KSO16 for 15" keyboard	For keyboard
35	03/13A	36	Delete BT_ON Pin34	For WLAN
36	03/13A	17、6	Change DDR to no interleave routing	For DDR
37	03/13B	36	Change LAN_WAKE# from UB1.108 to UB1.71	For EC
38	03/13B	36	Change WAKE# to EC_SWI# and connect to UB1.108	For EC
39	03/13B	34	Swap L60、L56、L71、L72	For DDR3
40	03/13B	37	Delete Q196	For WLAN LED
41	03/13B	35	Delete CA54、CA56	For Audio
42	03/13B	35	Swap JSPK	For Audio
43	03/14A	34	Swap LR7、LR8	For USB
44	03/14A	16、17	Swap JDDR3R、JDDR3S	For DDR
45	03/14B	33	Swap R44、R45、R46、R47	For Small board
46	03/14B	36	ADD JDB for EC debug	For Debug
47	03/14B	18	Change XTAL_OUTBUFF、XTAL_SSIN to RPV1.3、RPV1.4	For VGA
50	03/14B	18	Change SMB_CLK_GPU、SMB_DATA_GPU to RPV2.3、RPV2.4	For VGA
51	03/14B	16、17	JDDR3R、JDDR3S to JDDR3H、JDDR3L	For DDR
52	03/14B	31、36	ADD BT_ON	For WLAN
53	03/14B	36	EC_SMB_CK3、EC_SMB_DA3 change use 2.2K	For LVDS SM Bus
54	03/14B	10	Delete R307、R220	For Audio sleep & music
55	03/15A	5、10、37	Change CH7,D98,D99 BOM config from @ESD@ to ESD@	For ESD's request.
56	03/15A	36	Change CB14 BOM config from @ to ESD@ for ESD's request.	For ESD
57	03/15A	35	Delete RA50 for sleep & Music	For Audio
58	03/15A	35	Swap JSB5 and modify JSB4、JSB5 pin define	For Small board
59	03/18A	05	Change CH11 from 180PF to 100PF for ESD's request.	For ESD
60	03/18A	36	Change CB13 from 100PF to 0.1UF for ESD's request.	For ESD

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HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.0 TO 0.1

GERBER-OUT DATE: 2013/04/01

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
61	03/18A	10	Change CH7, CB14 from 180PF to 0.1UF for ESD's request.	For ESD
62	03/18A	37	Change D98,D99 to CH12, CH13 for ESD's request.	For ESD
63	03/19A	31	Modify JWLAN	For WLAN
64	03/19A	31	Modify JSB4 - JSB5 pin define & Add R49 - R50 - R53 - R51	For Small board
65	03/19B	33	Change JNGFF connector	For SSD
66	03/19B	29 - 28	Swap RP1 - RP2 - D97 - L61 - L62	For Layout
67	03/20A	37	R480 +5VS change to +5VALW	For WLAN
68	03/20A	33	Delete LR5(USB20_P2_L - USB20_N2_L), change to small board	For EMI
69	03/20B	33	JNGFF pin1 - pin13 - pin61 - pin67 connect to GND	For SSD
70	03/20B	21	Delete LV4 - RV32 - RV33 - RV34 - RV50 (N14MGL@)	For VGA
71	03/20C	28	Swap D97	For Layout
72	03/20D	31	Delete LED_WIMAX# - RM6 (didn't support WIMAX)	For WLAN
73	03/20D	37	Delete Q157 - R480 (didn't support WIMAX)	For WLAN
74	03/21A	28	Change U50 BOM config from IEDP@ to always mount.	For LVDS issue
75	03/21A	28	Change R436 BOM config from LVDS@ to @.	For LVDS issue
76	03/21A	28	Change R436 BOM config from LVDS@ to @.	For LVDS issue
77	03/21A	38	Change Q6(SB570020110) to Q5539A(SB00000EO10)	For Layout placement
78	03/21A	36	Add RR8 - RR9 then connected to CB0_WAKE# and LAN_WAKE#	For LAN_WAKE#
79	03/21A	36	Add EC_CB1 at pin97	For LAN_WAKE#
80	03/21A	33	Change U13,U15 from SA00004KB00 to SA00003TV00.	For power switch issue on Rosetta
81	03/21A	34	Add RR6 - RR7,change RR2 - RR3 14641@ to @	For USB Sleep and Charge
82	03/21A	36	Add RR6 then connected to CHG_CB0 and EC_CB0	For USB Sleep and Charge
83	03/21A	34	Add RB11 - RB13 on EC_CB0 - EC_CB1 then pull-high to +3VALW_PCH	For USB Sleep and Charge
84	03/21A	33	Modify JNGFF Config pin define and add SSD_Detect pin	For SSD
85	03/21A	10	R215 change to 10K pull high 3.3V,PROJECT_ID change to SSD_Detect	For SSD
86	03/25A	35	EC_MUTE_INT change to COMBO_GPI and add CA48(10u)	For Audio Combo jack
87	03/25A	36	Delete EC_MUTE_INT - RB38 - RB39	For Audio Combo jack
88	03/25A	33	Add test point	For SSD
89	03/25A	35	Add RA71 - change Combo jack GND to AGND - Change NBA_PLUG to NBA_PLUG#	For Audio
90	03/25A	35	Swap Q5539.3(NBA_PLUG) and Q5539.5(NBA_PLUG#)	For Audio
91	03/25A	35	change +MIC_VREFO to UA1.31	For Audio
92	03/25A	37	change ZZZ part number to DA8000Y0000	For Mother board location
93	03/25A	35	Add RA50 Reserve for solve noise issue	For Audio
94	03/25A	36	Add RB38 - RB39 fo Reserve solve S3 - S4 - S5 bo bo issue	For Audio
95	03/25A	31	JWLAN.42(CLK_EC) connect to U1H.AE6 for WLAN NGFF type use	For WLAN
96	03/25A	31	Delete pin64 - 66 net	For WLAN
97	03/25A	34	Change RB11,RB13 from un-mount to mount.	For Sleep & Charge
98	03/26A	10	ADD R30 for SSD detect	For SSD
99	03/26A	10	ADD RV32 for VRAM Strap pin	For VRAM
100	03/26A	32	Change JRJ45 footprint	For JRJ45
101	03/26A	37	H19 change to H_3P5x3P0N - H20 change to H_2P8N	For ME hole
102	03/26A	36	Delete RB5	For WLAN
103	03/26B	34	ADD RB5 Reserve for Seligo wake function	For USB switch
104	03/27A	34	Swap LR7	For Layout
105	03/27B	38	Change Q195 SB570020110 to SB00000DH00	For layout
106	03/27B	36	Delete RB38(EC_MUTE_INT_R)	For Audio
107	03/27B	38 - 35 - 34	Change Q195 - Q5539 - QR1 - Q5540 - SB00000EO10 to SB00000DH00	For X1 code
108	03/27B	18 - 8	Change QV1 - QV2 - QV4 - QV5 - QV7 - QV9 - QH4 SB00000EO10 to SB00000DH00	For X1 code
109	03/27B	29	Change Q190 - Q191 SB501110010 to SB00000PF00	For X1 code
110	03/27B	32	Change JRJ45 connector	For LAN
111	03/29A	37	H29 - H30 change to H_3P2 - ADD H7 H_3P0 - H13 change to H_3P5	For ME
112	03/29A	36	Delete RB39	For Audio
113	04/01A	35	ADD RA2 - MIC2_R_C_L - MIC2_R_C_R - MIC2_LINE1_R_L - MIC2_LINE1_R_R	For Audio 282 colay with 233
114	04/01A	35	Change +MIC1_VREFO(UA1.31) to +MIC2_VREFO(UA1.29)	For Audio
115	04/01A	35		

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ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2013/04/28

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	04/02A	29	ZZZ change to ZZZ1	For HDMI
2	04/02A	A11	Delete Footprint *NEW and *-NEW word	For Layout footprint
3	04/02A	35	ADD UA1 233@	For Audio
4	04/02A	21	ADD RV2 - CV115 - CV116 - CV117 and change RV1 - CV56 - CV32 - CV24 to ME@	For ME request
5	04/02A	21	ADD CV118 - CV119 - CV120 - CV121 and change CV28 - CV27 - CV29 - CV40 to ME@	For ME request
6	04/03A	19	ADD LV4 and change LV3 to ME@	For ME request
7	04/03A	35 - 36	ADD RA3 - EC_MUTE_INT connect to EC UB1.122	For Audio bobo noise issue
8	04/03A	35	RA62 change to @	For vendor request
9	04/03A	35	Delete RV2 - CV120 - CV121 and change to N14PGV2@	For Layout
10	04/03A	35	Change JRJ45 SANTA_130456-311 to SANTA_130456-491	For ME request
11	04/09A	36	Change UB1 Material SA000040B20 (A3) to SA000040B30 (A4)	For EC
12	04/09A	36	Change QB1 Material SB570020020 to SB000000EN00	For PUR cost request
13	04/09A	28	Change U50 Material SA007080100 to SA0000000H00	For Main source common
14	04/09A	35	Delete Q5539 - RA5	For Audio combo jack normal open
15	04/09A	33	Change NBA_PLUG to NBA_PLUG#	For Audio combo jack normal open
16	04/15A	22	Change RV54 33K to 4.7K	For +3VS_DGPU sequence faster
17	04/15A	35	Change LA8 KC_FBMA-10-100505-300T_2P to CHILI_SBY100505N-221Y-N_2P	For Layout
18	04/15A	37	Delete H12 and change H9 to H_4P0	For ME request
19	04/16A	31	ADD RC287 - RC288 - RC289 - RC290 - RC291 - RC292 - RC293 - RC294 - RC295	For mini PCIE WLAN
20	04/16A	31	ADD JWLAN1	For mini PCIE WLAN
21	04/16A	36	Delete UB1.26 FANPWM - ADD UB1.68 DFAN1	For FAN Control Circuit
22	04/16A	07	ADD U4 - C26 - R25 - C24 - C25 - C32 - Change JFAN	For FAN Control Circuit
23	04/16A	07	Delete R32 - C4 - R33 - D1 - C5	For FAN Control Circuit
24	04/16B	07	Delete RC292 - RC293 - ADD C161 - C163 - RC296 - RC297 - RC298 - RC299 - RC300	For mini PCIE WLAN
25	04/16B	07	ADD RC301 - RC302 -	For mini PCIE WLAN
26	04/16B	07	Change H8 H_5P0 to H_5P2	For ME hole
27	04/16C	07	Delete RC287 - RC302	For mini PCIE WLAN
28	04/18A	19	Delete LV4 - LV3 config change to OPT@	For mini PCIE WLAN
29	04/18A	35	Change LA8 Footprint to CHILI_SBY100505T-470Y-N_2P	For Audio
30	04/22A	31	JWLAN pin64 - 66 connect to +3V_WLAN	For WLAN
31	04/22A	36	UB1.89 CHG_PWR_GATE# change to ILIM_SEL	For USB sleep & charge
32	04/22A	34	Change USB sleep & charge chip to TPS2546RTER (Delete U5 - U14 - ADD UR4)	For USB sleep & charge
33	04/22A	34	Swap D87 - D88	For USB3.0 Layout
34	04/23A	34	Swap L56 - L60 - L71 - L72	For USB3.0 Layout
35	04/23B	35	ADD RA4 - RA5 75ohm	For Audio
36	04/23B	34	Swap LR7	For Layout
37	04/23B	07	U4 SA00002XA00 EOL change use SA00003UO00	For FAN
38	04/24A	37	H29 change to H_3P3 - H4 - H5 change to H_3P2	For ME modify
39	04/24B	31	ADD WLAN net name - C161 - C163 change to page 11	For WLAN
40	04/24B	34	UR4.5 USB_CHG_EN# change to USB_CHG_EN	For USB sleep & charge
41	04/24B	36	UB1.18 USB_CHG_EN# change to USB_CHG_EN	For USB sleep & charge
42	04/24B	36	CR10 4.7U_0805 change to 4.7U_0603 - ADD RR16 20K_0402_1%	For USB sleep & charge
43	04/24D	34	ADD CR8 - ILIM_SEL_R - CHG_CB0 - CHG_CB1 - EC_CHG_CB2	For USB sleep & charge
44	04/24D	35	Add CA49 - CA76 - CR8 - QA1 - RA6 - RA7 - RA72 - RA8 - LA9	For co-lay Audio 233/282/283
45	04/24D	35	Delete CA44 - Change CA7	For co-lay Audio 233/282/283
46	04/25A	35 - 36	Delete EC_MUTE_INT - RA3 - EC_MUTE_INT_R	For co-lay Audio 233/282/283 Line-in
47	04/25A	35	Add CA54 - CA55 - RA36 - RA37 - RA73 - RA74	For co-lay Audio 233/282/283 Line-in
48	04/26A	33	Add LR9 - LR10	For EMI request
49	04/26B	35	+LINE1_VREFO-R - +LINE1_VREFO-L change to +LINE1_VREFO_R - +LINE1_VREFO_L	For Audio
50	04/26C	33	Swap LR9 - LR10	For Layout
51	04/26C	35	Delete +LINE1_VREFO_R - +LINE1_VREFO_L - RA73 - RA36 - RA37 - CA54 - CA55	For no support Line-in
52	04/26C	35	Delete RA74	For no support Line-in
53	04/26D	19	Delete LV4	For Layout
54	04/26D	02	Modify Block Diagram	For Schematic
55	04/26E	32	Change UL2 material	For Cost request
56	04/26F	32	Delete R4283 - change PCIE_WAKE# to LAN_WAKE#	For LAN
57	04/26F	33	change SSD_Detect to SSD_DETECT# - ADD C4 - C5 - C6	For SSD
58	04/27G	32	Change UL2 material	For ME request
59	04/28A	35	Change Q5539B AGND to GND - Change title	For Audio
60	04/28A	33	Change title USB-CardReader Genesys GL834L to NGFF SATA/S_B conn/SPK	For Title
61	04/28B	08	RH66 0ohm change to 15ohm	For SPI EA report
62	04/29A	34	RR3 - RR4 change config to @ - Change UR4 to UR2 - Delete CR9	For USB sleep & charge

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HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2013/04/28

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
63	04/29B	10	Change R272 0603 to 0402	For EC

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	HW-PIR	
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ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2013/05/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01	05/02A	08	Delete R48、Y2、C2、C3	For Layout
02	05/02A	31	ADD CM6、CM8、CM7	For WLAN
03	05/03A	13	ADD C61、C69	For Customer request
04	05/03A	34	ADD RR17、Change RR@ config to @	For USB Sleep & charge
05	05/03A	36	ADD EC_CB2 to UB1.36	For USB Sleep & charge
06	05/03A	36	RB12 change config to @	For USB Sleep & charge
07	05/03A	35	Delete QA1B、Modify QA1A to QA1	For Audio
08	05/10A	08	ADD 10p at PCH_SPICLK for EA measure fail	For SPI ROM
09	05/10A	20	RV32 change N14PGV2@ to @	For Load BOM
10	05/16A	13	Delete C61	For Layout
11	05/16A	34	Update UR2 symbol	For USB sleep & charge
12	05/16B	31	Delete RC290、RC291	For Layout
13	05/16B	34	Swap LR8	For Layout
14	05/16C	34	RC298.1、RC298.1 net name swap、RC299.2、RC298.2 net name swap	For Layout
15	05/16C	34	JWLAN1.23 change net to PCIE_PRX_WLANTX_N4_R	For Layout
16	05/16C	34	JWLAN1.23 change net to PCIE_PRX_WLANTX_P4_R	For Layout
17	05/17A	33	Modify R46、R47、R44、R45、ADD LR11、LR12	For USB layout
18	05/17B	34	Delete RR15、RR10、RR12、RR11、RR13、RR17、RR2、RR3、RR4	For USB sleep & charge
19	05/17B	10	Delete SLP_CHG_CB1, CPU didn't need use	For USB sleep & charge
20	05/17C	33	Swap LR9、LR10	For JSB4
21	05/17E	34	Modify USB Sleep & charge table	For USB sleep & charge
22	05/20A	33	Swap LR9、LR10、LR11、LR12	For Layout
23	05/21A	07	Change JDB smybol	For Debug
24	05/21B	10	Change RP35 10K to 2.2K	For APU
26	05/23A	28	D16 LVDS@ config change to @、R433 Delete IEDP@ config	For LVDS
27	05/27A	34	C532、CR2 47U_0805 change to C535、C532、CR2、CR3 22u_0603	For ME layout request
28	05/27B	12	CC53 47U_0805 change to CC53、CC54 22u_0603	For ME layout request
29	05/27B	18、13	CV15、CV12、CV28、CV29、CV67 22U_0805 change to 22U_0603	For ME layout request
30	05/27B	36、37	EC_CB2(GPIO1A) move to GPIO12、ADD NUM_LED#(JKB5.1 to JUB1.36)	For Keyboard Number lock
31	05/29A	10、8	delete RH77, PCH_SMLDATA1 combine to RP35.4	For SMBUS
32	05/29A	10	change SML0CLK to RP35.1、SML0DATA to RP35.2、USB_OC#2 to RP34.5	For PU high resistor design
33	05/29A	37	add R480 & +3VS_NUM net	For Keyboard Number lock LED power
34	05/29A	31	change RCL2 from short pad to 33 Ohm	For 25M_LAN_LCK perormace
35	05/29B	9、32、29	add C489、C487	For ESD
36	05/29b	32	add DL4 & DL5, delete CL23 & CL24	For LAN ESD
37	05/30A	35	add RA9	For Audio 283 & 233
38	05/30b	38	add PJ333	For Cost down +1.5VALW to +1.5VS
40	05/31A	13	change R210 config to @, remove L3 config @	For +1.05VS_APLL0PI Power rail
41	05/31A	38	charnge R482、R483 from 10k to 100k	For reduce power consumption

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ZRMAA LA-A481P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 0.4

GERBER-OUT DATE: 2013/06/07

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01	06/06	08	Delete RH73 , PCH_SMLCLK1 combine to RP8	For part count reduce
02	06/06	08	add C71	For HDD cannot detect issue
03	06/06	11 ~ 31	change BOM , NonUltra@ to MWLAN@ ; Ultra@ to NWALN@	For modify correct BOM name
04	06/06	31	JWLAN.46 direct connect to BT_ON	For BT cannot turn off issue
05	06/06	31	move RM25 to JWLAN1.5	For BT cannot turn off issue
06	06/06A	31	add CCL10	For HDD cannot detect issue
07	06/07A		add R234	For OC# pull hing

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HW PIR (Product Improve Record)

ZRMAA LA-A481P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.4 TO 1.0
GERBER-OUT DATE: 2013/06/21

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01	06/14	08	RH42 0 ohm change to 22 ohm	For HDD cannot detect issue
02	06/14	35	RA45,RA46,RA42 short pad change to 0 ohm	For high frequency headphone zi zi noise when system idle.
03	06/14	31	RC298,RC299 change BOM , NWLN@ to MWLAN@	For SSD cannot detect issue
04	06/18	36	Add RB28	For audio EC_MUTE_INT common design
05	06/18	35	Change LA9 BOM config from EMI@ to 233@EMI@	For modify BOM config
06	06/20	34	Update USB3.0 conn footprint	For ME request
07	06/20	12 、 10 、 13	Delete T43, T32, T102	
08	06/20	9	add R418	For DP portB pull down
09	06/20	9 、 28	delete RH19 , add U51	For DOS mode garbage issue
10	06/21	7 、 9 、 31 、 33 、 36	change R65 、 R163 、 R471 、 R472 、 RB7 、 RC285 、 RCL5 、 RH26 footprint to short pad	For cost down
11	06/21	28	delete D16	For layout space concern
12	06/21	21	add LV4	For +PEX_PLLVDD Power ripple